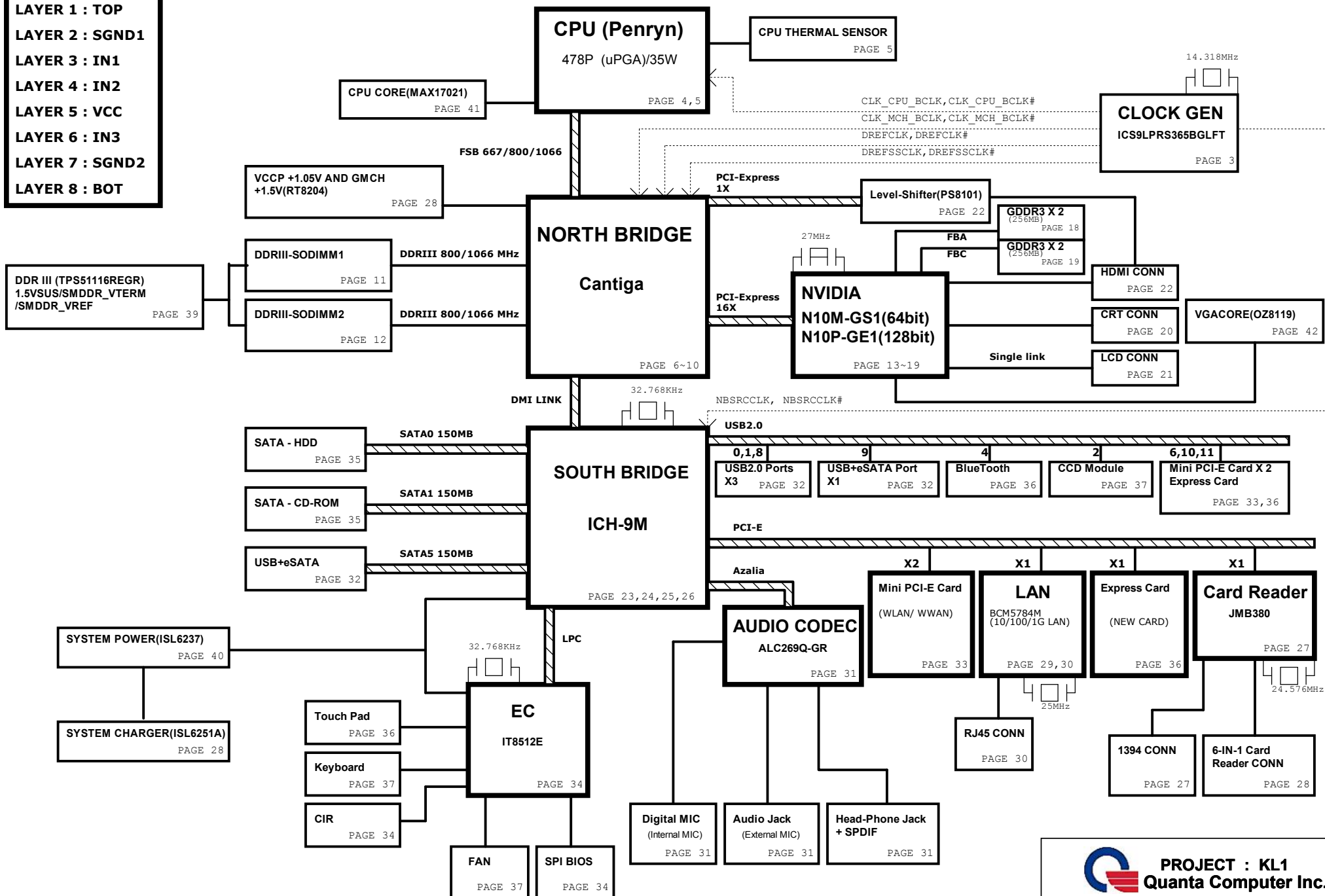


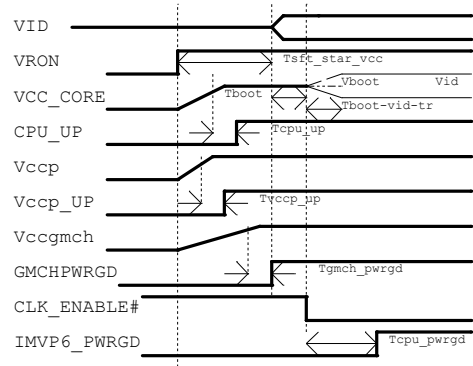
LAYER 4 : IN2
LAYER 5 : VCC
LAYER 6 : IN3
LAYER 7 : SGND2
LAYER 8 : BOT



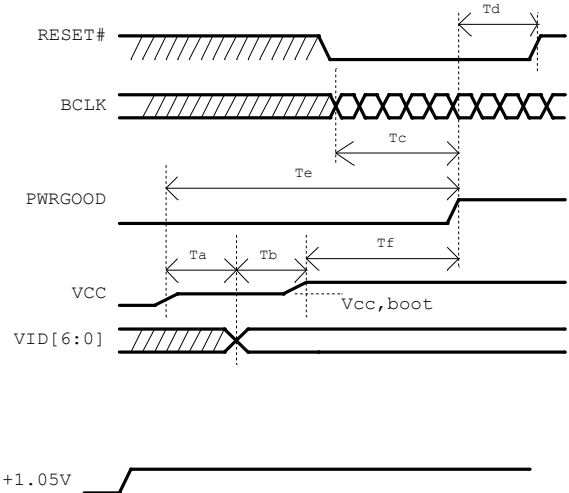
PCB Layers

Layer 1		TOP
Layer 2		GND
Layer 3		IN1
Layer 4		IN2
Layer 5		SVCC
Layer 6		IN3
Layer 7		GND
Layer 8		BOTTOM

Power On Sequencing Timing Diagram



Penryn Power-up Timing Specifications



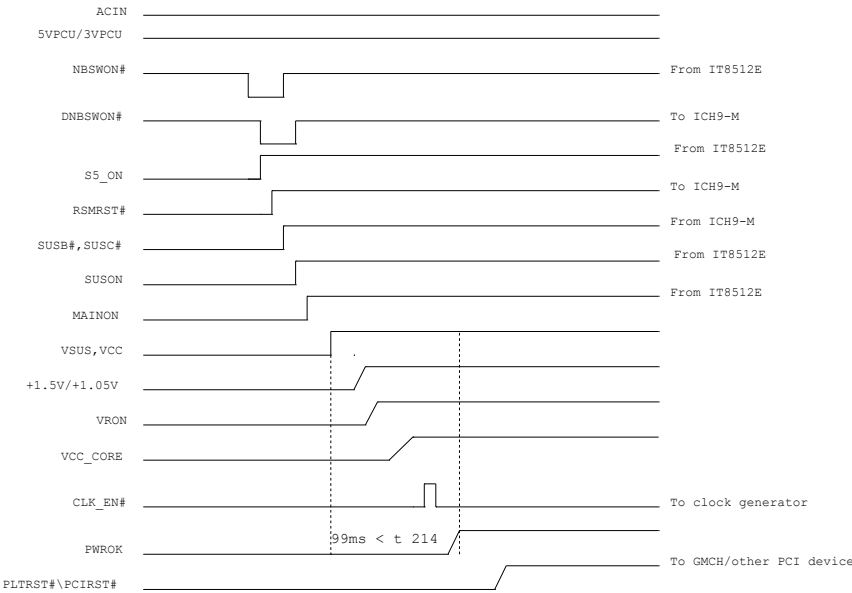
Ta=VCC and VCCP asseration to VID[6:0] vaild
Tb=VID[6:0] stable to VCC vaild
Tc=BCLK stable to PWRGOOD asseration
Td=PWRGOOD to RESET# de-asseration time
Te=VCC not vaild to PWRGOOD asseration time


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Voltage Rails

Voltage Rails	ON S0-S2	ON S3	ON S4	ON S5	Control signal
VCC_CORE	V				VRON
+1.5V	V				MAINON
+1.05V	V				MAINON
5V_S5/3V_S5	V	V	V	V	S5_ON
5VSUS/3VSUS/1.5VSUS	V	V			SUSON
SMDRR_VTERM/+3V/+5V/+15V/+1.8V	V				MAINON
+VGACORE/+VGA1.1V	V				MAINON
LANVCC	V	V			LAN_ON
3VPCU	V	V	V	V	VL
5VPCU	V	V	V	V	VL

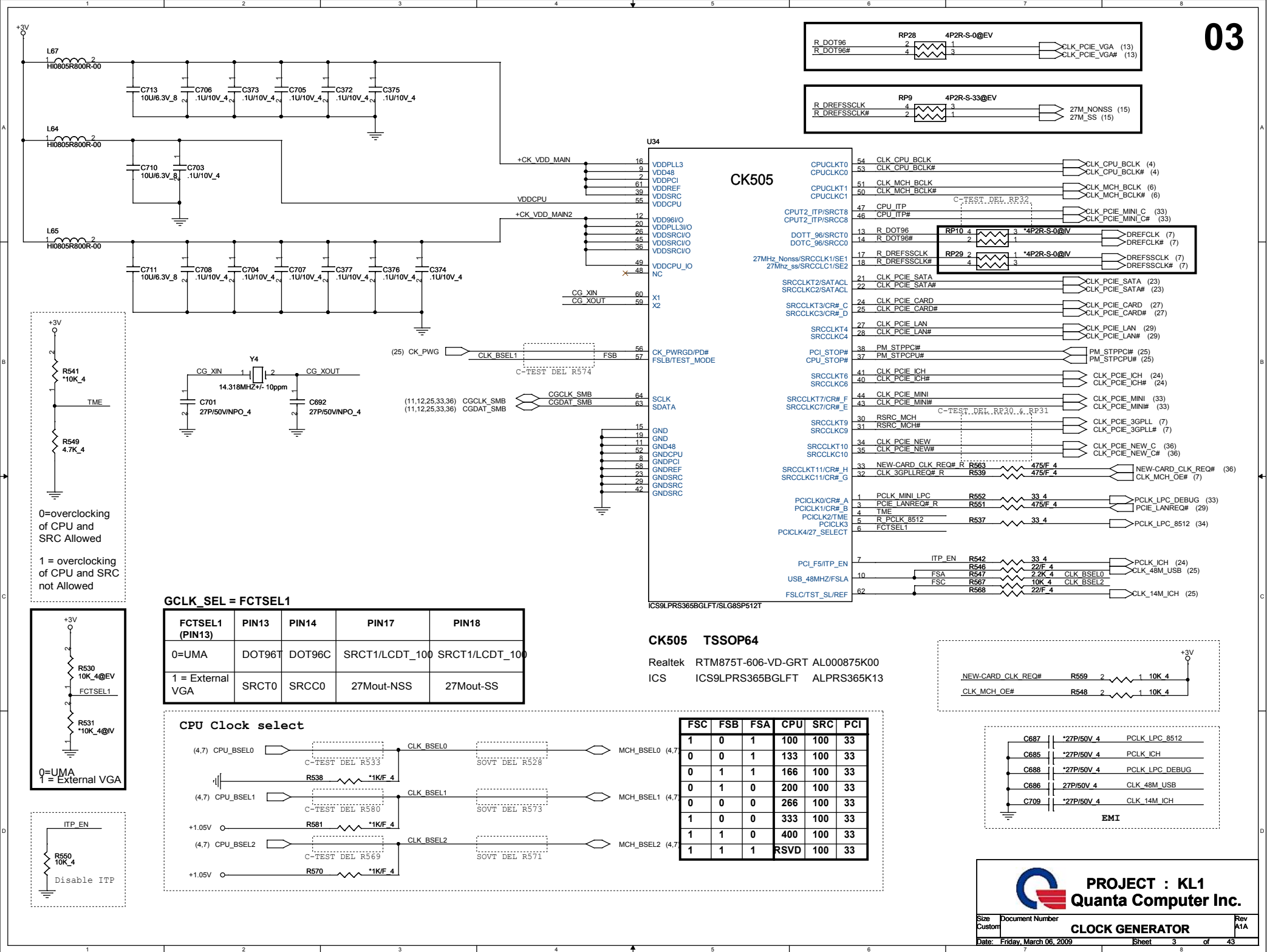
ACIN POWER ON TIMING



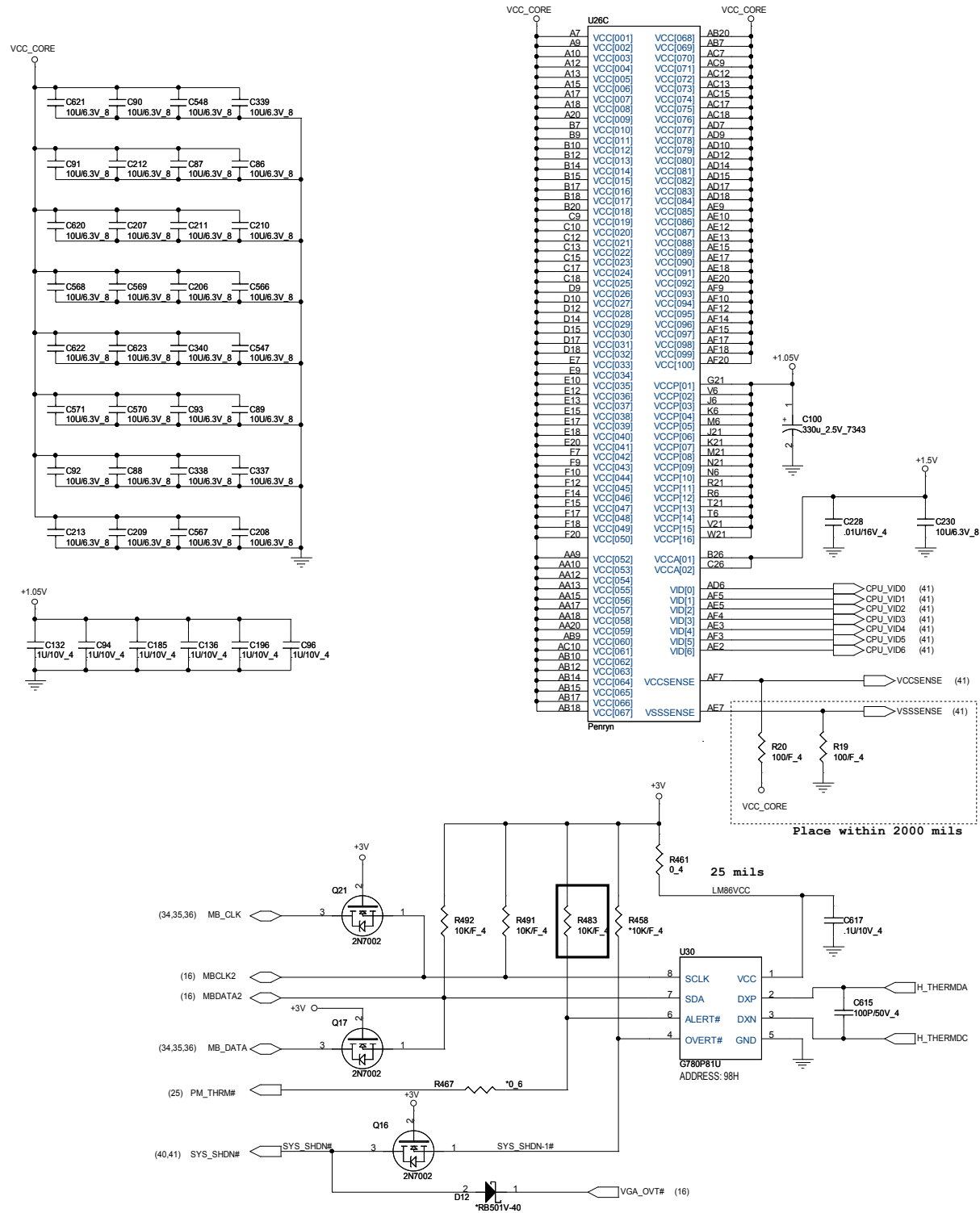


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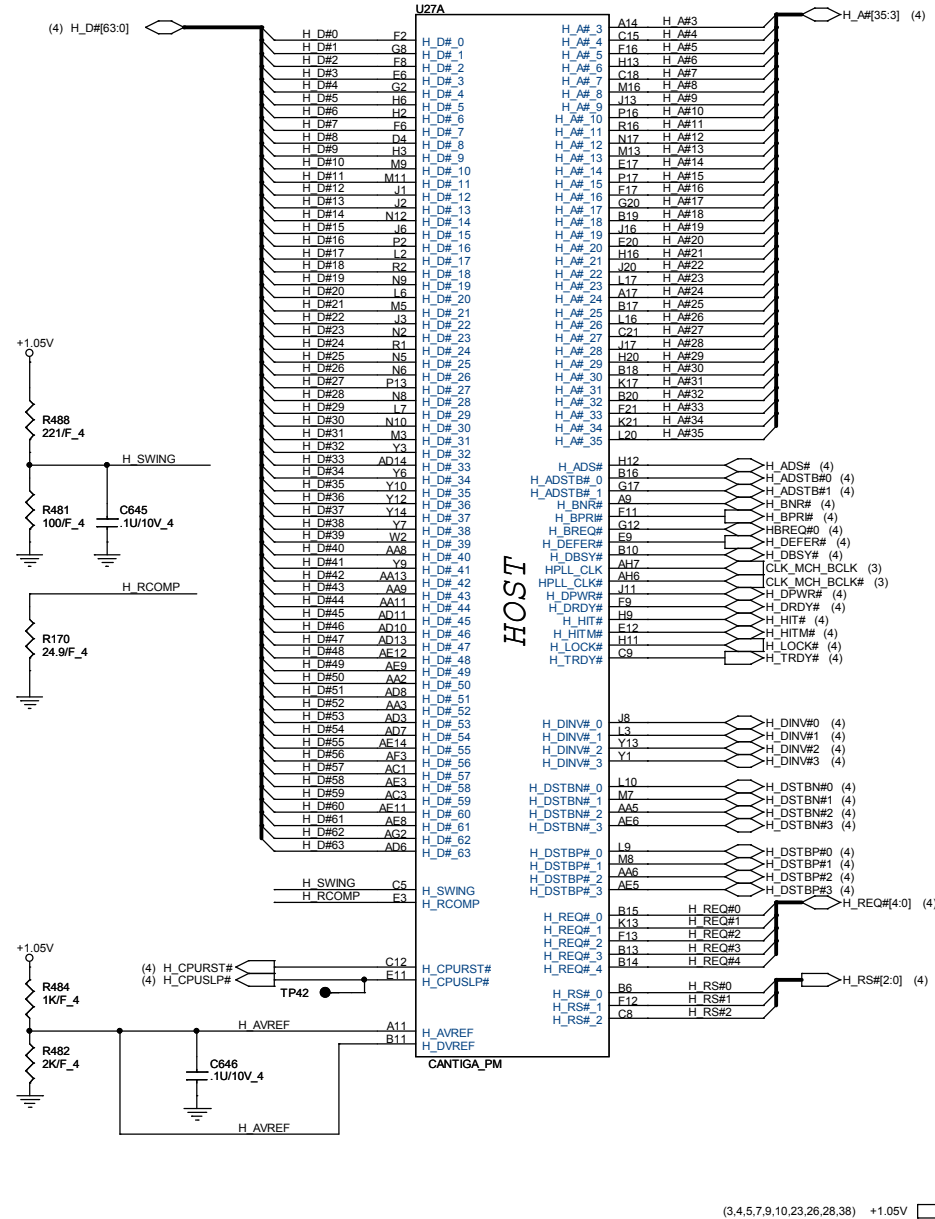
Size Custom	Document Number	SYSTEM INFORMATION	Rev A1A
Date: Friday, March 06, 2009	Sheet 2 of 43		





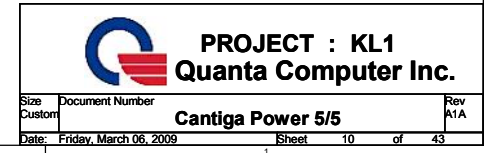


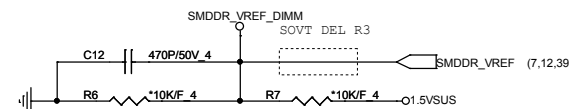
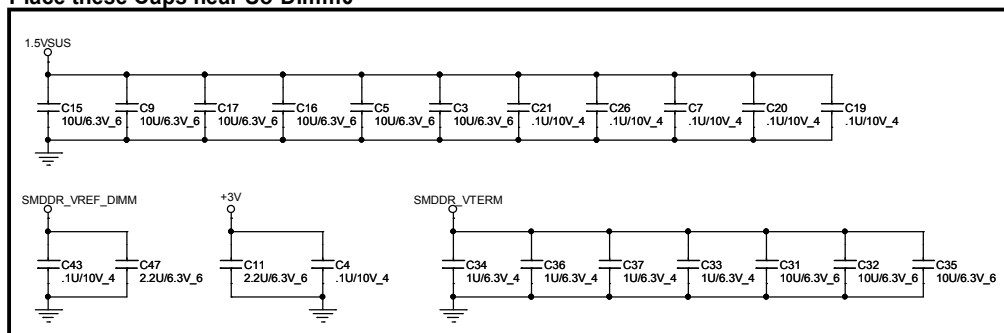
U26D		
A4	VSS[001]	P6
A5	VSS[002]	P21
A11	VSS[003]	P24
A14	VSS[004]	R2
A16	VSS[005]	R5
A19	VSS[006]	R22
A23	VSS[007]	R25
A23	VSS[008]	T1
B6	VSS[009]	T4
B8	VSS[010]	T23
B11	VSS[011]	T26
B13	VSS[012]	T3
B16	VSS[013]	U6
B19	VSS[014]	U21
B21	VSS[015]	U24
B24	VSS[016]	V2
C5	VSS[017]	V5
C8	VSS[018]	V22
C11	VSS[019]	V25
C14	VSS[020]	W1
C16	VSS[021]	W4
C19	VSS[022]	W23
C2	VSS[023]	W26
C22	VSS[024]	Y3
C25	VSS[025]	Y6
D1	VSS[026]	Y21
D4	VSS[027]	Y24
D11	VSS[028]	AA2
D13	VSS[029]	AA5
D16	VSS[030]	AA11
D19	VSS[031]	AA14
D23	VSS[032]	AA16
D26	VSS[033]	AA19
E3	VSS[034]	AA22
E6	VSS[035]	AA25
E8	VSS[036]	AB1
E11	VSS[037]	AB4
E14	VSS[038]	AB8
E16	VSS[039]	AB11
E19	VSS[040]	AB13
E21	VSS[041]	AB15
E24	VSS[042]	AB19
F5	VSS[043]	AB23
F11	VSS[044]	AB26
F13	VSS[045]	AC3
F16	VSS[046]	AC6
F19	VSS[047]	AC11
F2	VSS[048]	AC14
F22	VSS[049]	AC16
F25	VSS[050]	AC19
G4	VSS[051]	AC21
G1	VSS[052]	AC24
G23	VSS[053]	AD2
G26	VSS[054]	AD5
H3	VSS[055]	AD8
H6	VSS[056]	AD11
H21	VSS[057]	AD13
H24	VSS[058]	AD16
J2	VSS[059]	AD19
J5	VSS[060]	AD22
J22	VSS[061]	AD25
J25	VSS[062]	AE1
VSS[063]	VSS[063]	AE4
VSS[064]	VSS[064]	AE11
K1	VSS[065]	AE14
K4	VSS[066]	AE16
K23	VSS[067]	AE19
K26	VSS[068]	AE23
L3	VSS[069]	AE26
L6	VSS[070]	A2
L24	VSS[071]	AF6
M2	VSS[072]	AF8
M5	VSS[073]	AF11
M25	VSS[074]	AF13
N1	VSS[075]	AF16
N4	VSS[076]	AF19
N23	VSS[077]	AF21
N26	VSS[078]	A25
P3	VSS[079]	AF25
VSS[080]	VSS[080]	
VSS[081]	VSS[081]	

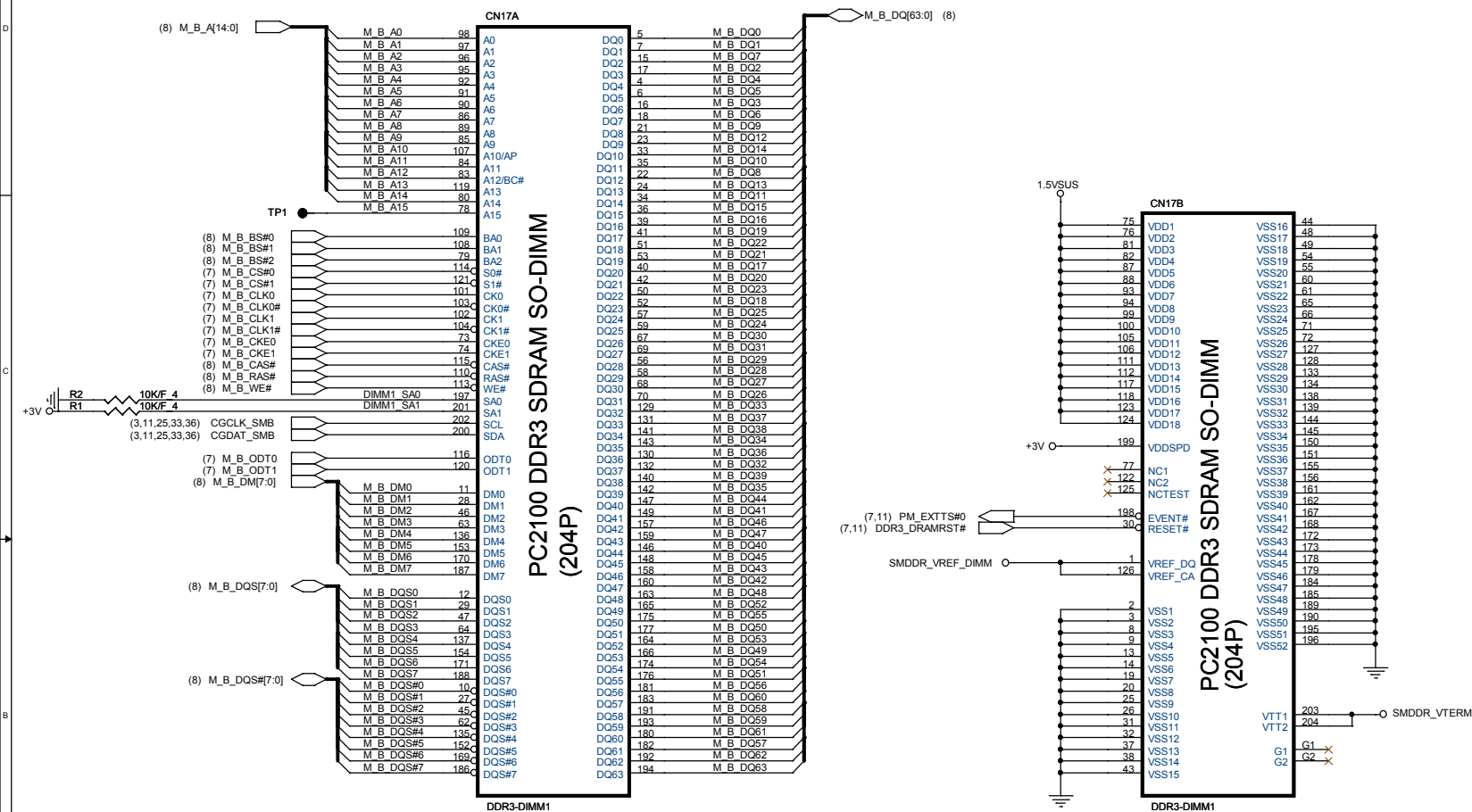




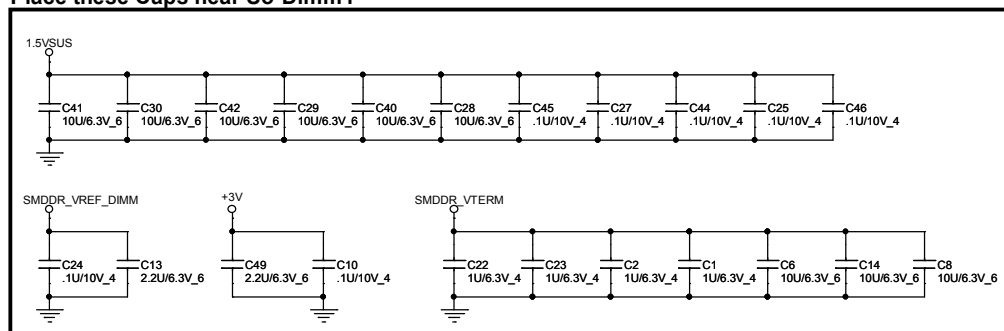


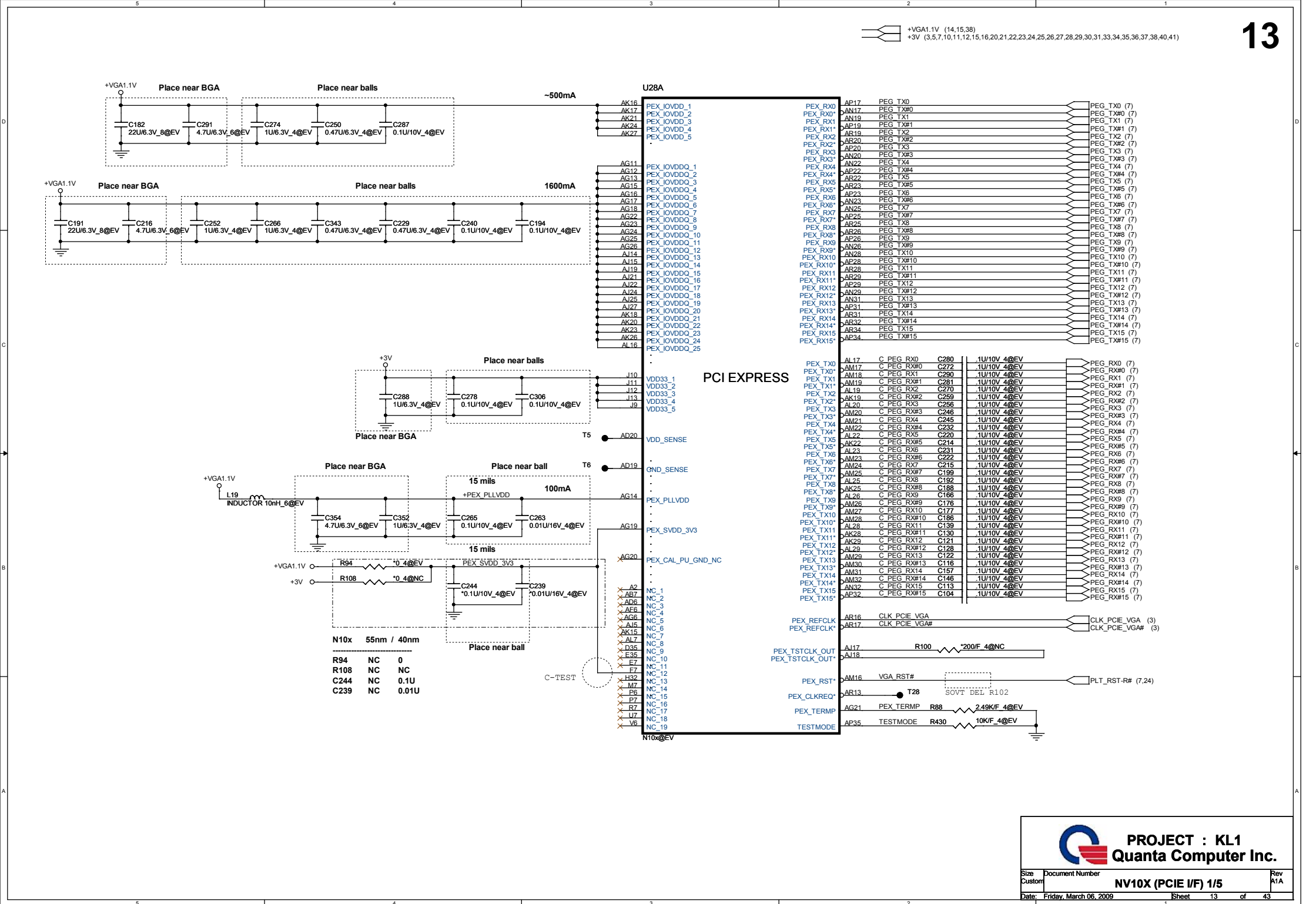






Place these Caps near So-Dimm1

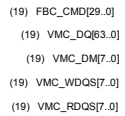




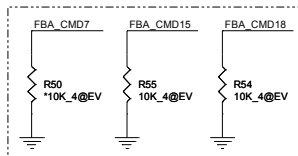
U28B

MEMORY I/F A

FBA_CMD0	V32	FBA_CMD0	FBA_D00	L32	VMA_D00
FBA_CMD1	W61	FBA_CMD1	FBA_D01	N33	VMA_D01
FBA_CMD2	U81	FBA_CMD2	FBA_D02	L33	VMA_D02
FBA_CMD3	Y32	FBA_CMD3	FBA_D03	N34	VMA_D03
FBA_CMD4	AB34	FBA_CMD4	FBA_D04	N35	VMA_D04
FBA_CMD5	AB34	FBA_CMD5	FBA_D05	P35	VMA_D05
FBA_CMD6	W35	FBA_CMD6	FBA_D06	P33	VMA_D06
FBA_CMD7	W33	FBA_CMD7	FBA_D06	P34	VMA_D07
FBA_CMD8	W30	FBA_CMD8	FBA_D07	K35	VMA_D08
FBA_CMD9	T34	FBA_CMD9	FBA_D08	K33	VMA_D09
FBA_CMD10	T35	FBA_CMD10	FBA_D09	K34	VMA_D010
FBA_CMD11	AB31	FBA_CMD11	FBA_D10	H33	VMA_D011
FBA_CMD12	Y31	FBA_CMD12	FBA_D11	G34	VMA_D012
FBA_CMD13	Y34	FBA_CMD13	FBA_D12	G33	VMA_D013
FBA_CMD14	W32	FBA_CMD14	FBA_D13	E34	VMA_D014
FBA_CMD15	AA30	FBA_CMD15	FBA_D14	E33	VMA_D015
FBA_CMD16	AA32	FBA_CMD16	FBA_D15	G31	VMA_D016
FBA_CMD17	Y33	FBA_CMD17	FBA_D16	F30	VMA_D017
FBA_CMD18	U32	FBA_CMD18	FBA_D17	G30	VMA_D018
FBA_CMD19	Y31	FBA_CMD19	FBA_D18	G32	VMA_D019
FBA_CMD20	U34	FBA_CMD20	FBA_D19	K30	VMA_D020
FBA_CMD21	Y34	FBA_CMD21	FBA_D20	K32	VMA_D021
FBA_CMD22	W34	FBA_CMD22	FBA_D21	H30	VMA_D022
FBA_CMD23	V30	FBA_CMD23	FBA_D22	K31	VMA_D023
FBA_CMD24	U35	FBA_CMD24	FBA_D23	L31	VMA_D024
FBA_CMD25	U30	FBA_CMD25	FBA_D24	L30	VMA_D025
FBA_CMD26	U33	FBA_CMD26	FBA_D25	M32	VMA_D026
FBA_CMD27	AB30	FBA_CMD27	FBA_D26	N30	VMA_D027
FBA_CMD28	AB33	FBA_CMD28	FBA_D27	M30	VMA_D028
FBA_CMD29	W29	FBA_CMD29	FBA_D28	P31	VMA_D029
FBA_CMD30	W29	FBA_CMD30	FBA_D29	R32	VMA_D030
FBA_CMD31	P32	FBA_CMD31	FBA_D30	R30	VMA_D031
FBA_CMD32	H34	FBA_CMD32	FBA_D31	R30	VMA_D032
FBA_CMD33	I30	FBA_CMD33	FBA_D32	AG30	VMA_D033
FBA_CMD34	P30	FBA_CMD34	FBA_D33	AG32	VMA_D034
FBA_CMD35	AF32	FBA_CMD35	FBA_D34	AH31	VMA_D035
FBA_CMD36	AL32	FBA_CMD36	FBA_D35	AF31	VMA_D036
FBA_CMD37	AL34	FBA_CMD37	FBA_D36	AF30	VMA_D037
FBA_CMD38	AF35	FBA_CMD38	FBA_D37	AC32	VMA_D038
FBA_CMD39	AF35	FBA_CMD39	FBA_D38	AD30	VMA_D039
FBA_CMD40	AF35	FBA_CMD40	FBA_D39	AM33	VMA_D040
FBA_CMD41	AF35	FBA_CMD41	FBA_D40	AL31	VMA_D041
FBA_CMD42	AF35	FBA_CMD42	FBA_D41	AM33	VMA_D042
FBA_CMD43	AF35	FBA_CMD43	FBA_D42	AL33	VMA_D043
FBA_CMD44	AF35	FBA_CMD44	FBA_D43	AK30	VMA_D044
FBA_CMD45	AF35	FBA_CMD45	FBA_D44	AK32	VMA_D045
FBA_CMD46	AF35	FBA_CMD46	FBA_D45	AJ30	VMA_D046
FBA_CMD47	AF35	FBA_CMD47	FBA_D46	AH30	VMA_D047
FBA_CMD48	AF35	FBA_CMD48	FBA_D47	AH33	VMA_D048
FBA_CMD49	AF35	FBA_CMD49	FBA_D48	AH35	VMA_D049
FBA_CMD50	AF35	FBA_CMD50	FBA_D49	AH34	VMA_D050
FBA_CMD51	AF35	FBA_CMD51	FBA_D50	AH32	VMA_D051
FBA_CMD52	AF35	FBA_CMD52	FBA_D51	AJ33	VMA_D052
FBA_CMD53	AF35	FBA_CMD53	FBA_D52	AL35	VMA_D053
FBA_CMD54	AF35	FBA_CMD54	FBA_D53	AM34	VMA_D054
FBA_CMD55	AF35	FBA_CMD55	FBA_D54	AM35	VMA_D055
FBA_CMD56	AF35	FBA_CMD56	FBA_D55	AE33	VMA_D056
FBA_CMD57	AF35	FBA_CMD57	FBA_D56	AE32	VMA_D057
FBA_CMD58	AF35	FBA_CMD58	FBA_D57	AF34	VMA_D058
FBA_CMD59	AF35	FBA_CMD59	FBA_D58	AE35	VMA_D059
FBA_CMD60	AF35	FBA_CMD60	FBA_D59	AE34	VMA_D060
FBA_CMD61	AF35	FBA_CMD61	FBA_D60	AE33	VMA_D061
FBA_CMD62	AF35	FBA_CMD62	FBA_D61	AB32	VMA_D062
FBA_CMD63	AF35	FBA_CMD63	FBA_D62	AC35	VMA_D063



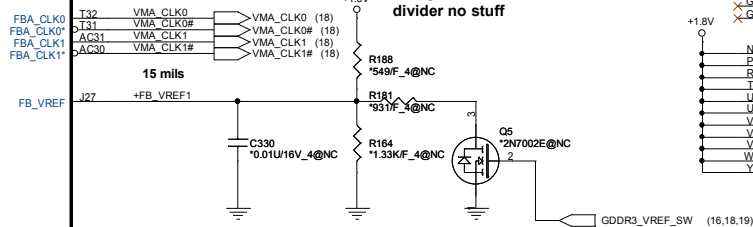
+1.8V (15,18,19,28,37,38)
+VGA1.1V (13,15,38)



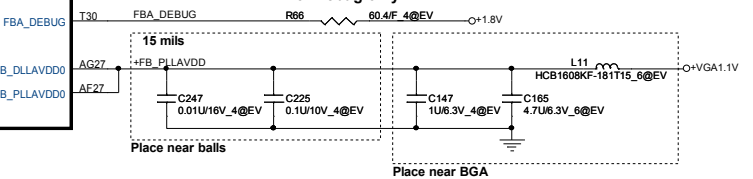
N10x 55nm / 40nm

R50	NC	10K
R55	10K	10K
R54	10K	10K

Using internal Vref, ext
divider no stuff



For Debug only



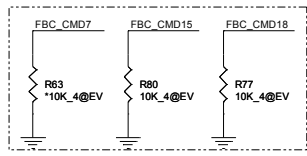
Place near balls

Place near BGA

U28C

MEMORY I/F B

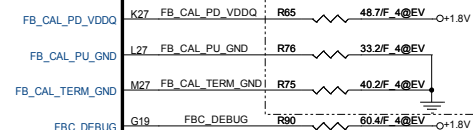
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FBC_CMD1	B19	FBC_CMD1	FBC_D01	D13	VMC_D01
FBC_CMD2	D18	FBC_CMD2	FBC_D02	A13	VMC_D02
FBC_CMD3	F21	FBC_CMD3	FBC_D03	A14	VMC_D03
FBC_CMD4	A23	FBC_CMD4	FBC_D04	C16	VMC_D04
FBC_CMD5	D21	FBC_CMD5	FBC_D05	B16	VMC_D05
FBC_CMD6	B23	FBC_CMD6	FBC_D06	A17	VMC_D06
FBC_CMD7	E20	FBC_CMD7	FBC_D07	D16	VMC_D07
FBC_CMD8	G21	FBC_CMD8	FBC_D08	C13	VMC_D08
FBC_CMD9	F20	FBC_CMD9	FBC_D09	B11	VMC_D09
FBC_CMD10	C19	FBC_CMD10	FBC_D10	C11	VMC_D010
FBC_CMD11	F23	FBC_CMD11	FBC_D11	A11	VMC_D011
FBC_CMD12	A22	FBC_CMD12	FBC_D12	C10	VMC_D012
FBC_CMD13	C22	FBC_CMD13	FBC_D13	B8	VMC_D014
FBC_CMD14	B17	FBC_CMD14	FBC_D14	A8	VMC_D015
FBC_CMD15	F24	FBC_CMD15	FBC_D15	E8	VMC_D016
FBC_CMD16	C25	FBC_CMD16	FBC_D16	F10	VMC_D018
FBC_CMD17	D22	FBC_CMD17	FBC_D17	F19	VMC_D019
FBC_CMD18	B22	FBC_CMD18	FBC_D18	F12	VMC_D020
FBC_CMD19	A19	FBC_CMD19	FBC_D19	D8	VMC_D021
FBC_CMD20	A19	FBC_CMD20	FBC_D20	D11	VMC_D022
FBC_CMD21	D20	FBC_CMD21	FBC_D21	E11	VMC_D023
FBC_CMD22	E19	FBC_CMD22	FBC_D22	D12	VMC_D024
FBC_CMD23	D19	FBC_CMD23	FBC_D23	E13	VMC_D026
FBC_CMD24	D19	FBC_CMD24	FBC_D24	F13	VMC_D027
FBC_CMD25	F18	FBC_CMD25	FBC_D25	F14	VMC_D028
FBC_CMD26	F18	FBC_CMD26	FBC_D26	F16	VMC_D028
FBC_CMD27	F18	FBC_CMD27	FBC_D27	F16	VMC_D030
FBC_CMD28	F18	FBC_CMD28	FBC_D28	F17	VMC_D031
FBC_CMD29	F18	FBC_CMD29	FBC_D29	F17	VMC_D032
FBC_CMD30	F18	FBC_CMD30	FBC_D30	F27	VMC_D034
FBC_CMD31	F18	FBC_CMD31	FBC_D31	F28	VMC_D035
FBC_CMD32	F18	FBC_CMD32	FBC_D32	F28	VMC_D037
FBC_CMD33	F18	FBC_CMD33	FBC_D33	F28	VMC_D038
FBC_CMD34	F18	FBC_CMD34	FBC_D34	F28	VMC_D039
FBC_CMD35	F18	FBC_CMD35	FBC_D35	F28	VMC_D040
FBC_CMD36	F18	FBC_CMD36	FBC_D36	F28	VMC_D041
FBC_CMD37	F18	FBC_CMD37	FBC_D37	F28	VMC_D042
FBC_CMD38	F18	FBC_CMD38	FBC_D38	F28	VMC_D043
FBC_CMD39	F18	FBC_CMD39	FBC_D39	F28	VMC_D044
FBC_CMD40	F18	FBC_CMD40	FBC_D40	F28	VMC_D045
FBC_CMD41	F18	FBC_CMD41	FBC_D41	F28	VMC_D046
FBC_CMD42	F18	FBC_CMD42	FBC_D42	F28	VMC_D047
FBC_CMD43	F18	FBC_CMD43	FBC_D43	F28	VMC_D048
FBC_CMD44	F18	FBC_CMD44	FBC_D44	F28	VMC_D049
FBC_CMD45	F18	FBC_CMD45	FBC_D45	F28	VMC_D050
FBC_CMD46	F18	FBC_CMD46	FBC_D46	F28	VMC_D051
FBC_CMD47	F18	FBC_CMD47	FBC_D47	F28	VMC_D052
FBC_CMD48	F18	FBC_CMD48	FBC_D48	F28	VMC_D053
FBC_CMD49	F18	FBC_CMD49	FBC_D49	F28	VMC_D054
FBC_CMD50	F18	FBC_CMD50	FBC_D50	F28	VMC_D055
FBC_CMD51	F18	FBC_CMD51	FBC_D51	F28	VMC_D056
FBC_CMD52	F18	FBC_CMD52	FBC_D52	F28	VMC_D057
FBC_CMD53	F18	FBC_CMD53	FBC_D53	F28	VMC_D058
FBC_CMD54	F18	FBC_CMD54	FBC_D54	F28	VMC_D059
FBC_CMD55	F18	FBC_CMD55	FBC_D55	F28	VMC_D060
FBC_CMD56	F18	FBC_CMD56	FBC_D56	F28	VMC_D061
FBC_CMD57	F18	FBC_CMD57	FBC_D57	F28	VMC_D062
FBC_CMD58	F18	FBC_CMD58	FBC_D58	F28	VMC_D063
FBC_CMD59	F18	FBC_CMD59	FBC_D59	F28	VMC_D064
FBC_CMD60	F18	FBC_CMD60	FBC_D60	F28	VMC_D065
FBC_CMD61	F18	FBC_CMD61	FBC_D61	F28	VMC_D066
FBC_CMD62	F18	FBC_CMD62	FBC_D62	F28	VMC_D067
FBC_CMD63	F18	FBC_CMD63	FBC_D63	F28	VMC_D068



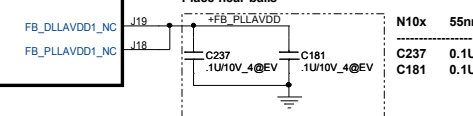
N10x 55nm / 40nm

R63	NC	10K
R80	10K	10K
R77	10K	10K

N10x-55nm for GDDR3



Place near balls



N10x 55nm / 40nm

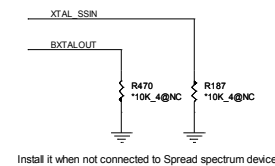
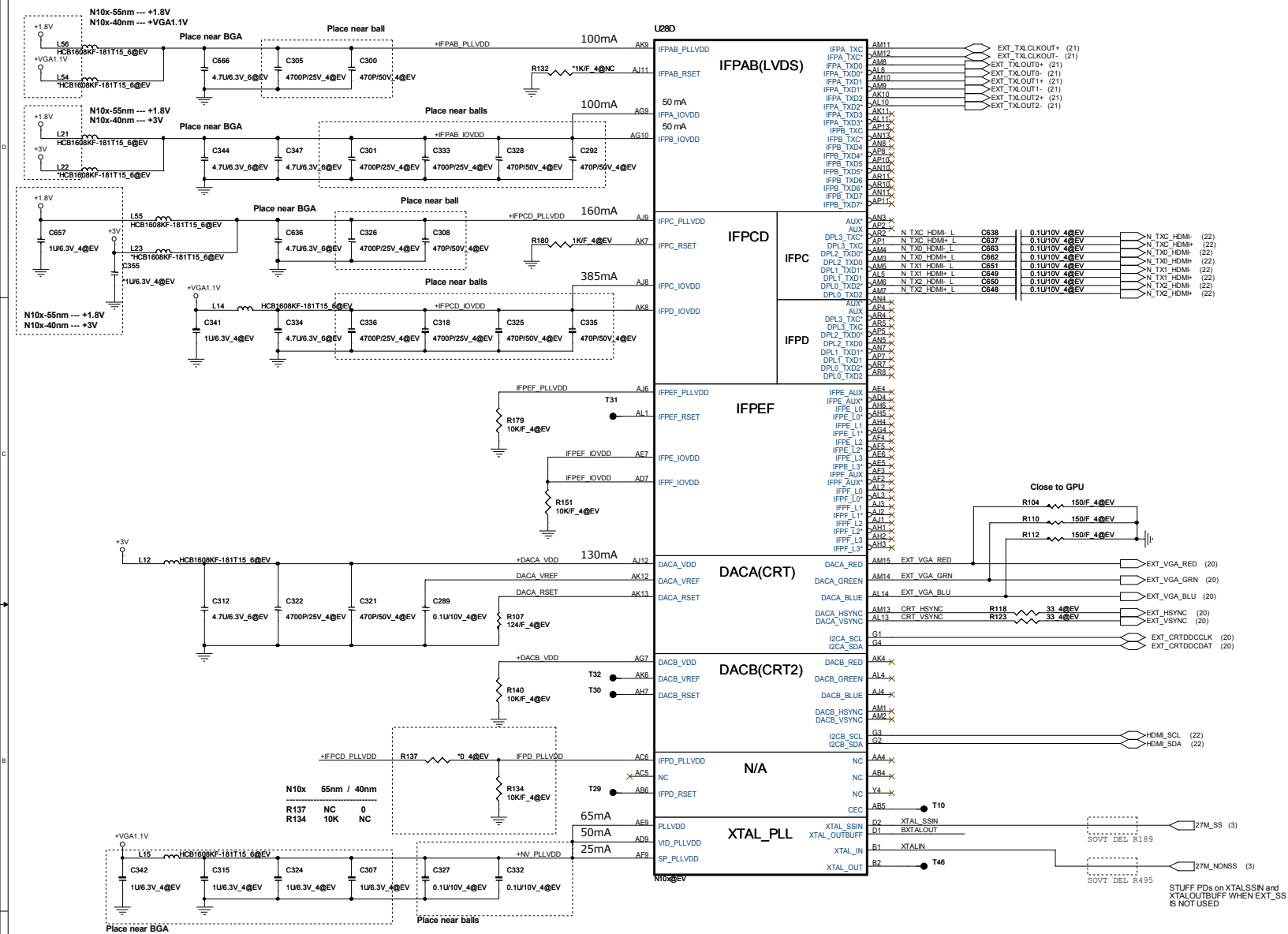
C237	0.1U	NC
C181	0.1U	NC

Signal Name	N10M-55nm N10P-55nm	N10M-40nm N10P-40nm
FBCAL_PD_VDDQ	48.7 ohm	GDDR3
FBCAL_PU_GND	33.2 ohm	
FBCAL_TERM_GND	40.2 ohm	



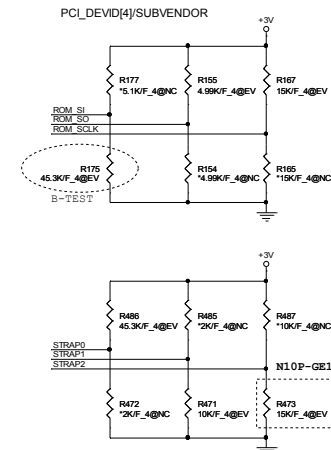
PROJECT : KL1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	NV10X (MEMORY I/F) 2/5	A1A
Date:	Friday, March 06, 2009	Sheet 14 of 43



N10P-GE1 Straps
N10M-GS1 Straps
GPIO ASSIGNMENTS

GPI/O	I/O	ACTIVE	USAGE
0	IN	N/A	PRIMARY DVI HOTPLUG
1	IN	N/A	SECONDARY DVI HOTPLUG
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	N/A	NVDD VID0
6	OUT	N/A	NVDD VID1
7	OUT	N/A	FBVDD VID0
8	IN	LOW	THERMAL ALERT
9	OUT	LOW	FAN PWM
10	OUT	N/A	FBVREF SELECT
11	OUT	N/A	SLI SYNC0
12	IN	N/A	AC DETECT
13	OUT	LOW	PS CONTROL OR HDMI_CEO
14	OUT	HIGH	PS CONTROL



N10P-GE1 55nm / 40nm		N10M-GS1 55nm / 40nm	
R167	15K/F	R167	15K/F
R165	NC	R165	NC
R487	NC	R487	NC
R473	15K/F	R473	10K/F

Logical Strap Bit Mapping

5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

STRAP TABLE

```

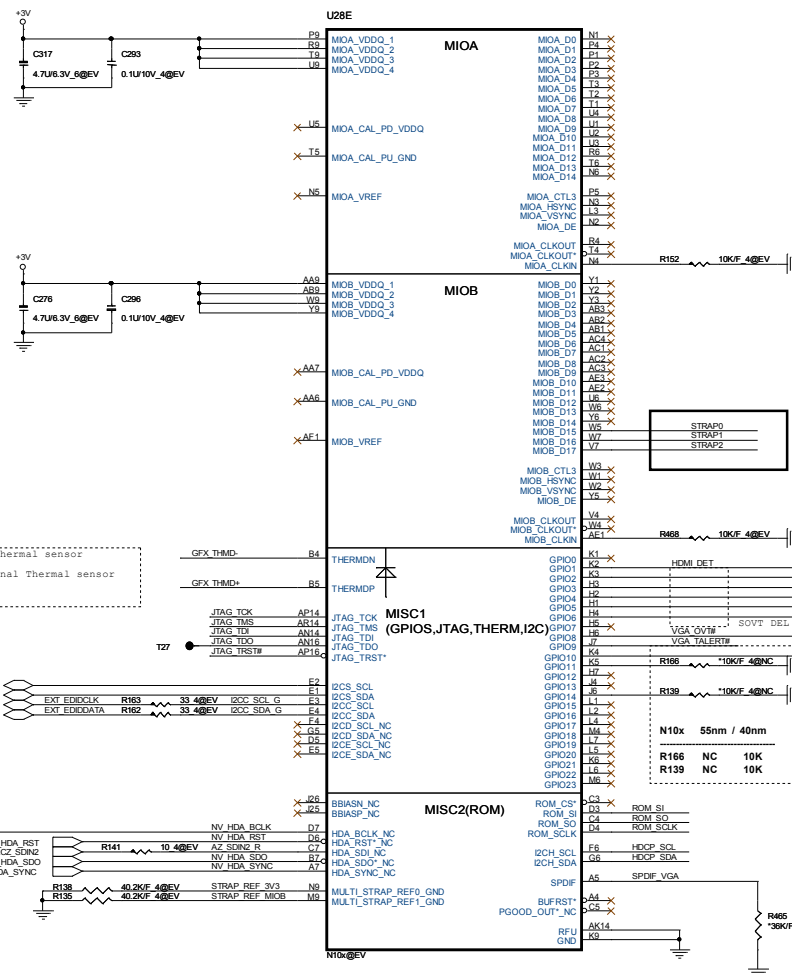
STRAP0: USER[3:0]
STRAP1: 3GIO PADCFG[3:0]
STRAP2: PCI DEVID[3:0]
ROM SCLK: PCI DEVID EXT, SUB VENDOR, SLOT CLK CFG, FEX PLL EN TERM
ROM SI: RAMCFG[3:0]
ROM SO: XCLK 417, FB 0 BAR SIZE, SMB ALT ADDR, VGA DEVICE

```

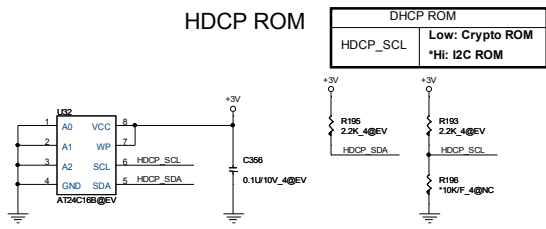
KL1 STRAP FUNCTION MAPPING

```
USER[3:0]: 1111
3GIO PADCFG[3:0]: 0001 NoteBook
PCI DEVID[3:0]: 0001
SUB_VENDOR: 0 No Vedio BIOS ROM
SLOT CLK CLG: 1 GPU AND MCH USE COMMON REF CLOCK
PEX PLL EN TERM: 0 DISABLE PEX PLL TERMINATION
RAMCFG[3:0]: 0000 AND 0001
XCLK_417: 1 USING 27MHz
FB 0 BAR SIZE:
SMB ALT ADDR:
VGA DEVICE:
```

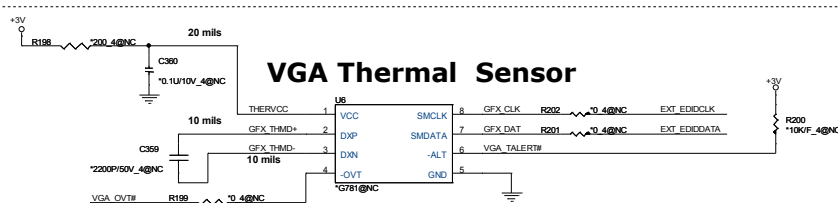
ROM SI	RAMCFG LSIT:		
PD R175:45K/F	0111	SAMSUNG K4J10324QD-HC12	32M32b * 4PCS
PD R175:30K/F	0101	QIMONDA HYB18H1G321AF-11	32M32b * 2PCS



HDCP ROM

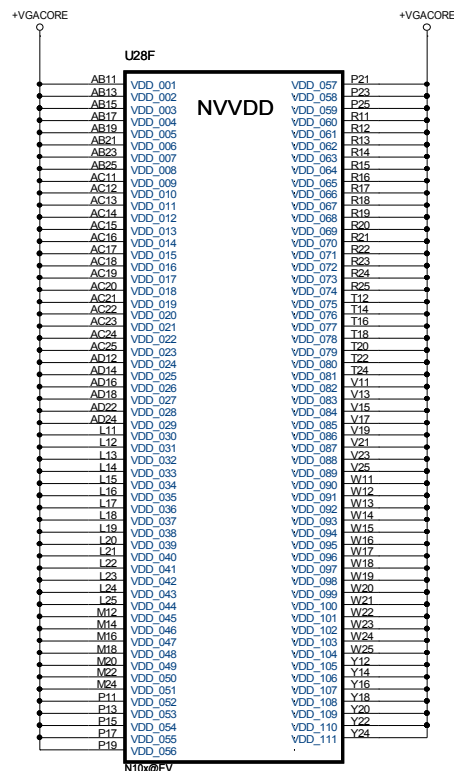


VGA Thermal Sensor

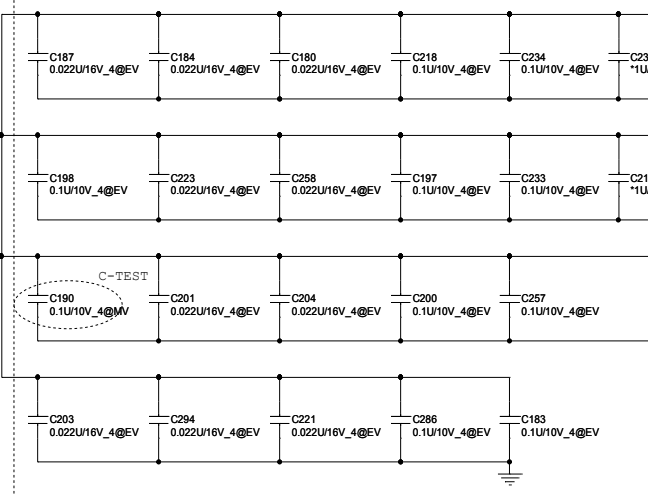


Use 100% GuaiGNP Trace around THERMDC and THERMDA

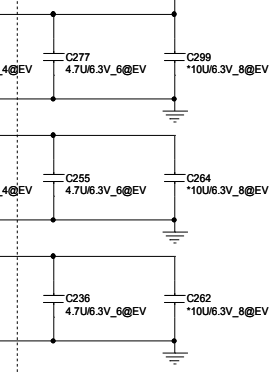
NVVDD Decoupling



Place near balls



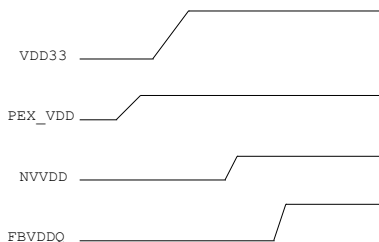
Place near BGA



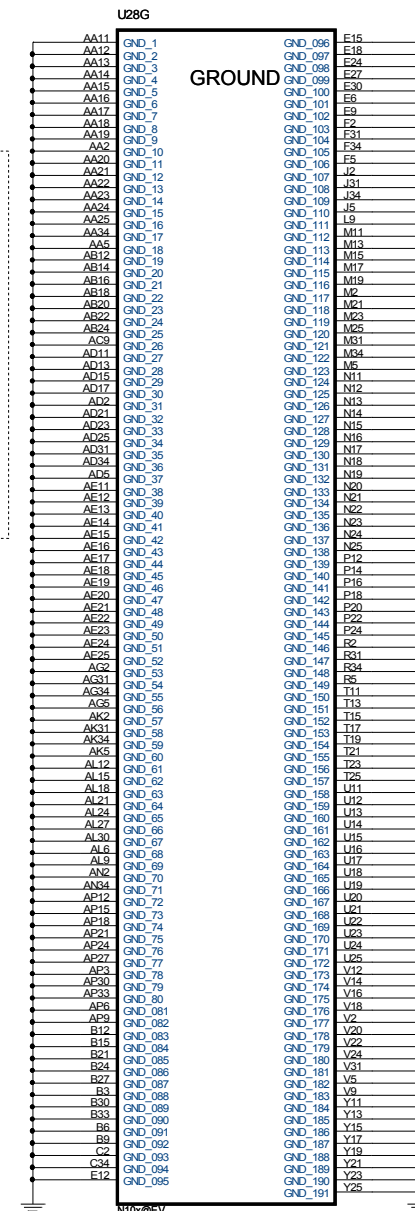
N10x	55nm	40nm
C187	0.022U	0.01U
C198	0.1U	0.01U
C190	0.1U	0.01U
C235	NC	1U
C217	NC	1U
C277	4.7U	1U
C255	4.7U	4.7U
C236	4.7U	NC
C299	NC	10U
C264	NC	10U
C262	NC	10U

N10P-GE1: +VGACORE +0.90V (Normal)

power up sequence

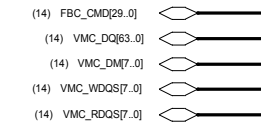


+VGACORE (37,38,42)



PROJECT : KL1
Quanta Computer Inc.





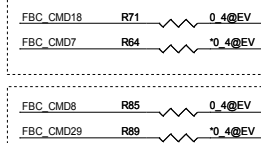
Group 2: D16~D23

Group 3: D24~D31

Group 0: D0~D7

Group 1: D8~D15

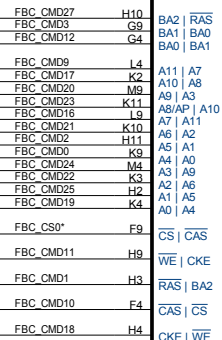
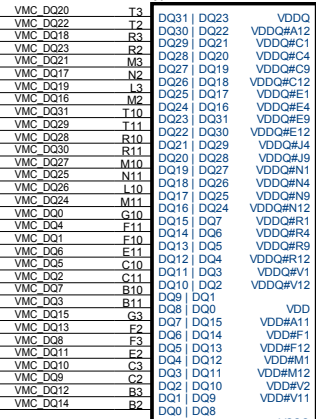
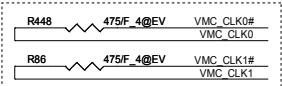
N10x	55nm	40nm
DQ	0..31	32..63
QAE0	A4	RA5
QAE1	RA5	RA5
QAE2	A5	A5
QAE3	BA1	BA1
QAE4	A2	A2
QAE5	A4	A4
QAE6	A3	A3
QAE7	CS1*	CS1*
QAE8	CS0*	CS0*
QAE9	A11	A11
QAE10	QAS*	QAS*
QAE11	WE*	WE*
QAE12	BA0	BA0
QAE13	A5	A5
QAE14	A12	A12
QAE15	RETC0*	RETC0*
QAE16	A7	A7
QAE17	A10	A10
QAE18	CKE	CKE
QAE19	A8	A8
QAE20	A8	A8
QAE21	A8	A8
QAE22	A2	A2
QAE23	A8	A8
QAE24	A3	A3
QAE25	A1	A1
QAE26	A13	A13
QAE27	BA2	BA2
QAE28		QDRCS1*
QAE29	CS0*	
QAE30	QDRCS1*	



N10x 55nm / 40nm

R71	0	NC
R64	NC	0
R85	0	NC
R89	NC	0

Place near VRAM side

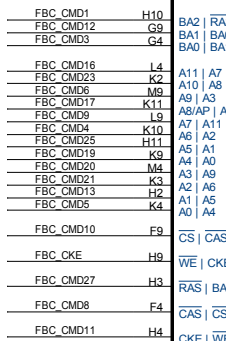
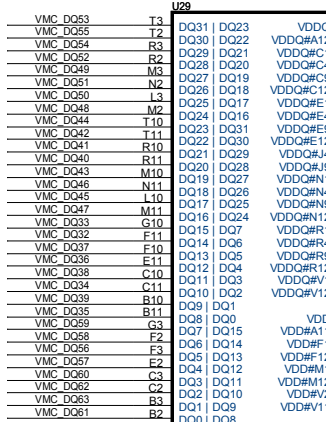
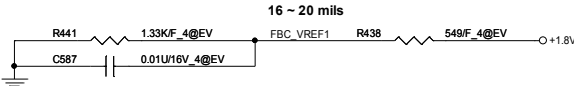
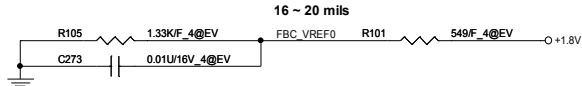
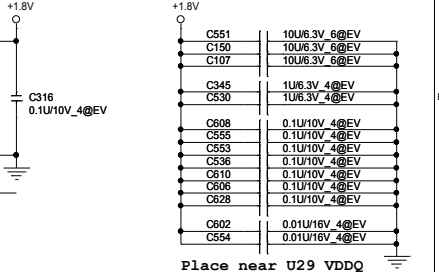
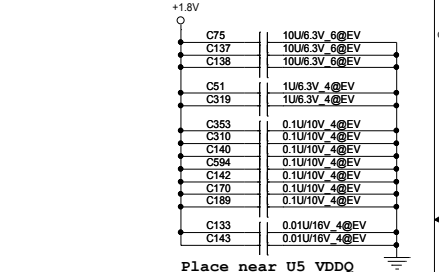
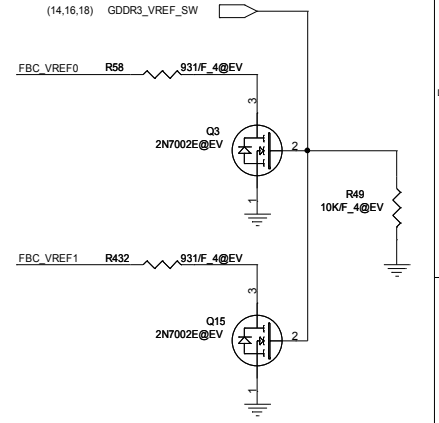
QIMONDA: HYB18H1G321AF-11
SAMSUNG: K4J10324QD-HC12

Group 6: D48~D55

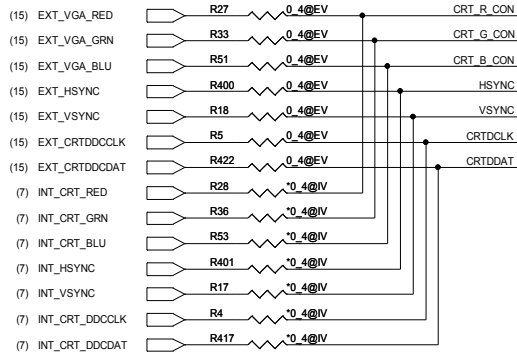
Group 5: D40~D47

Group 4: D32~D39

Group 7: D56~D63

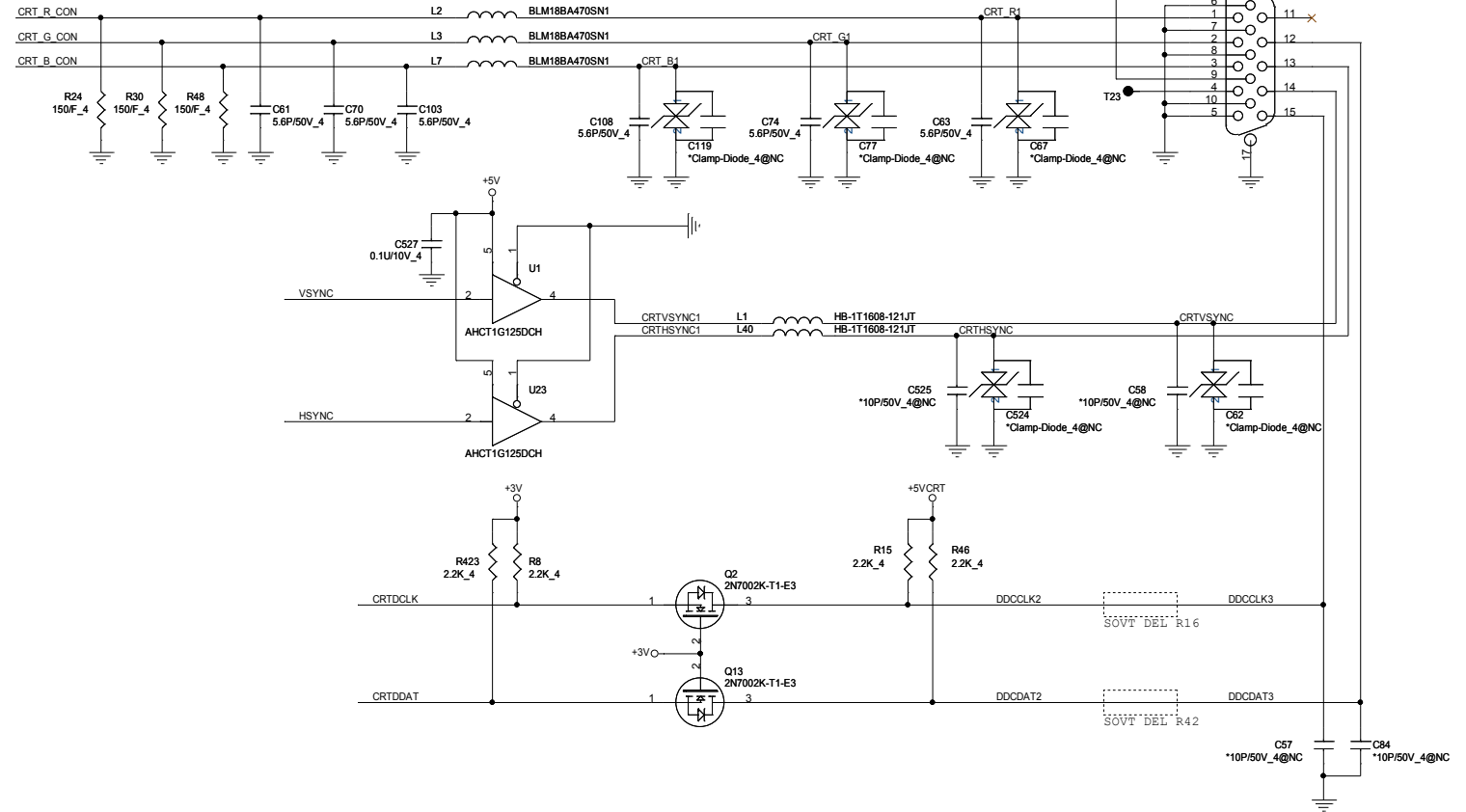
QIMONDA: HYB18H1G321AF-11
SAMSUNG: K4J10324QD-HC12

CRT SWITCH



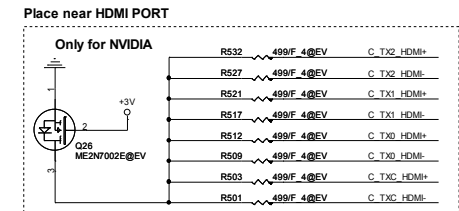
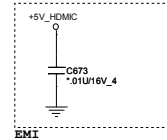
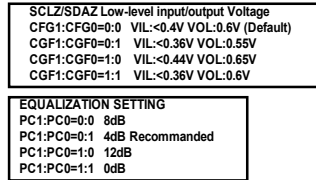
UMA & Discrete setting
LVDS Discrete / UMA

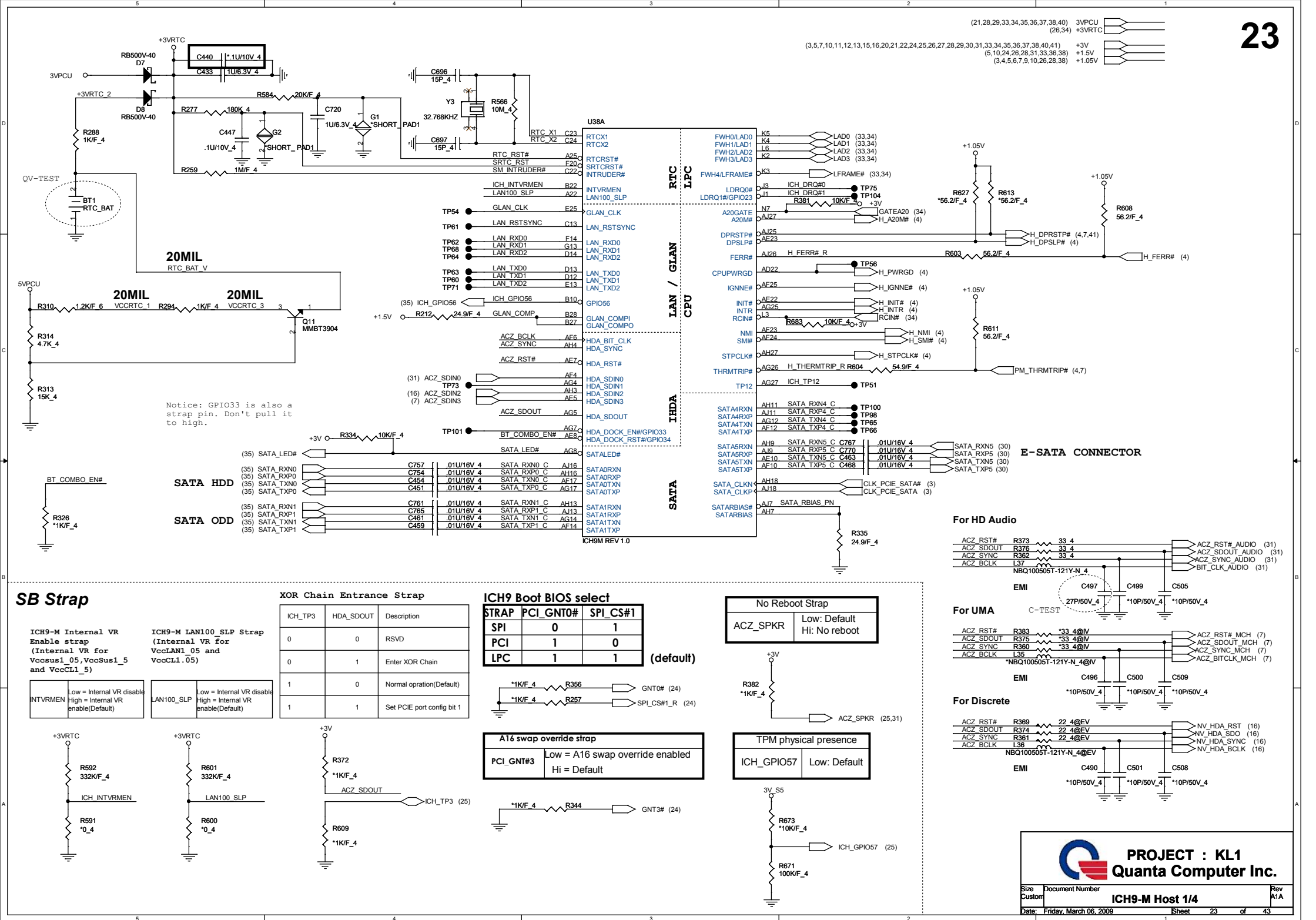
R27	0	NC
R33	0	NC
R51	0	NC
R400	0	NC
R18	0	NC
R5	0	NC
R422	0	NC
R28	NC	0
R36	NC	0
R53	NC	0
R401	NC	0
R17	NC	0
R4	NC	0
R417	NC	0

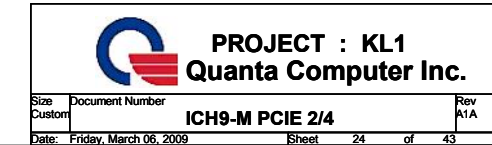


PROJECT : KL1
Quanta Computer Inc.

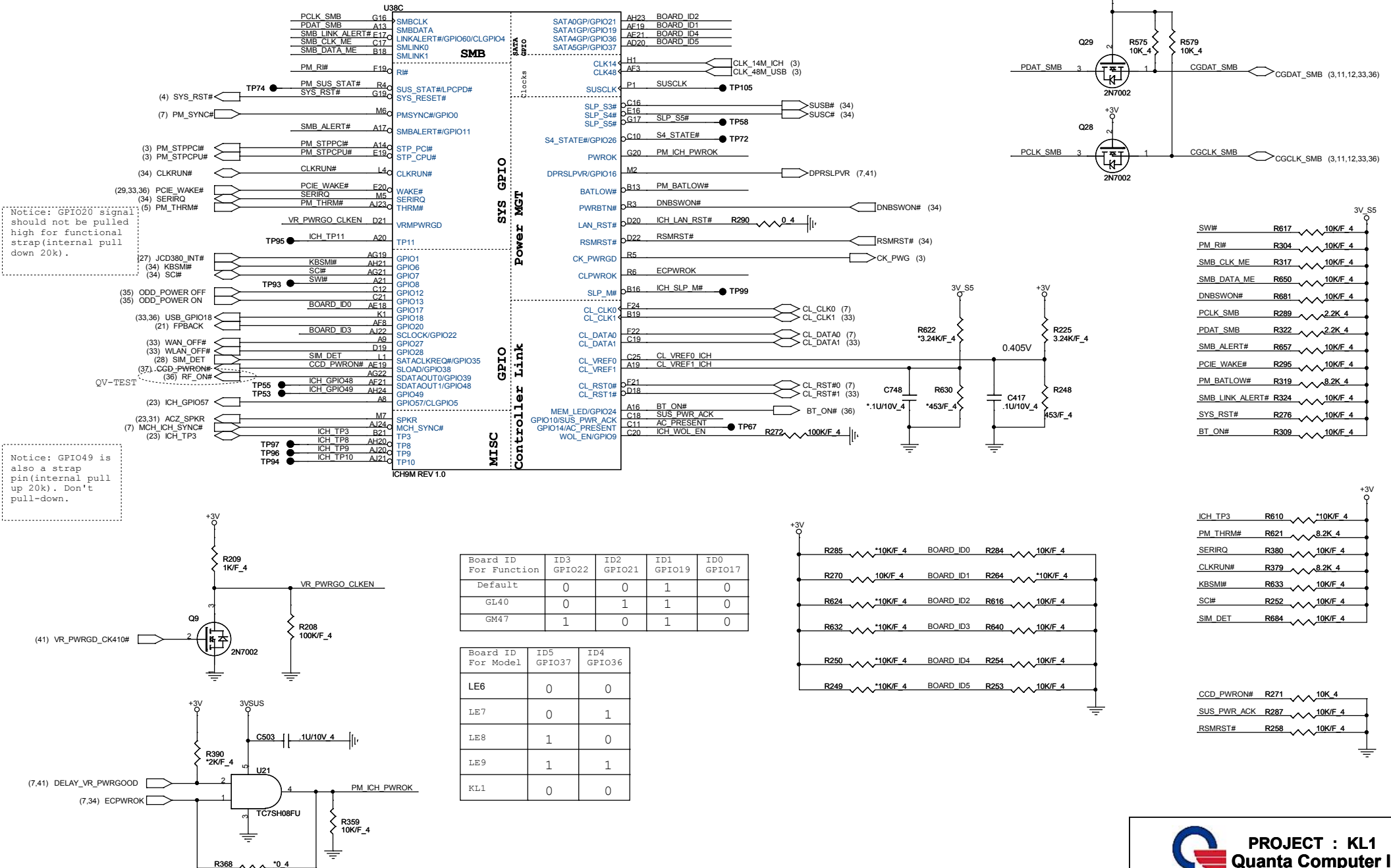
Size Custom Document Number CRT CONN Rev A1A
Date: Friday, March 06, 2009 Sheet 20 of 43







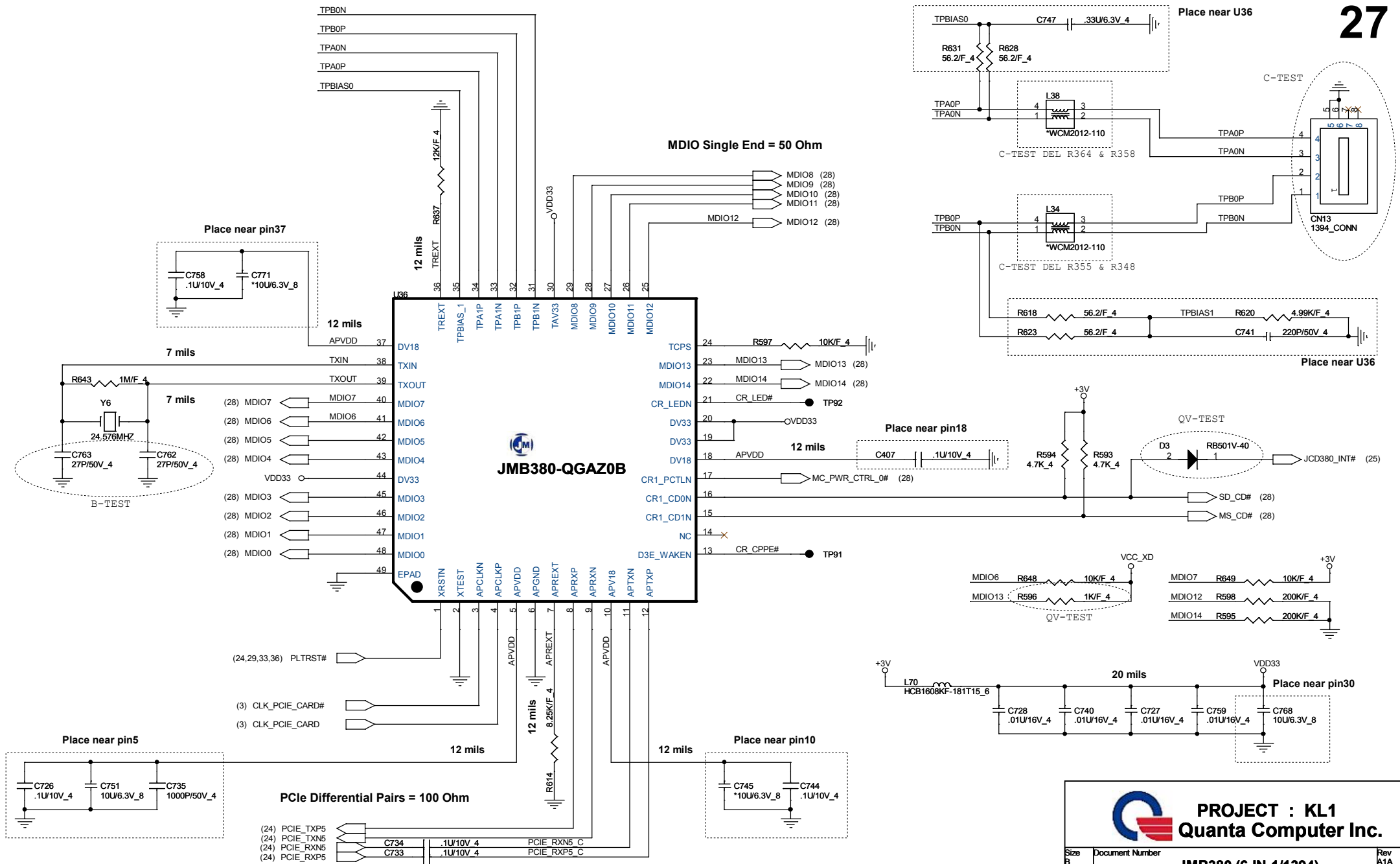
(3,5,7,10,11,12,13,15,16,20,21,22,23,24,26,27,28,29,30,31,33,34,35,36,37,38,40,41) +3V
(23,24,26,38) 3V_S5
(33,34,36,38,39,41,42) 3VSUS

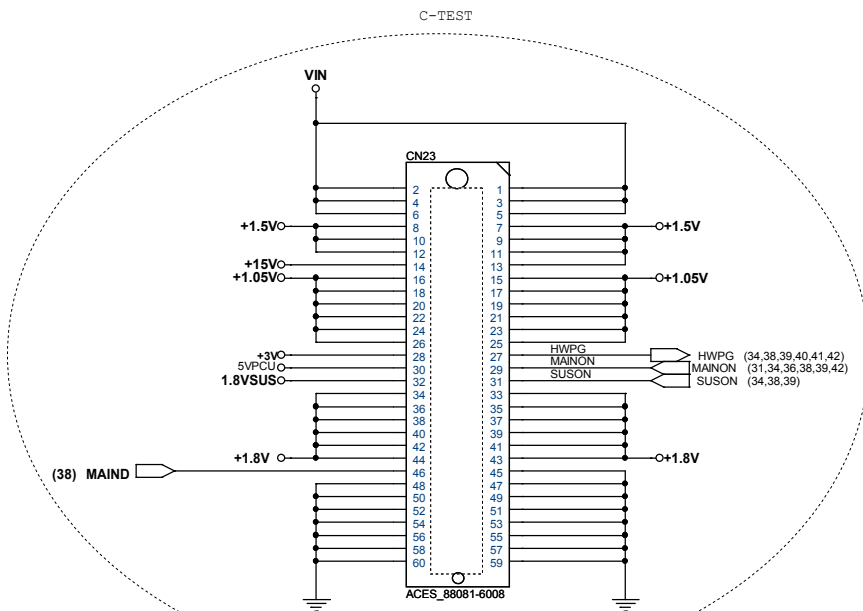


Board ID For Function	ID3 GPIO22	ID2 GPIO21	ID1 GPIO19	ID0 GPIO17
Default	0	0	1	0
GL40	0	1	1	0
GM47	1	0	1	0

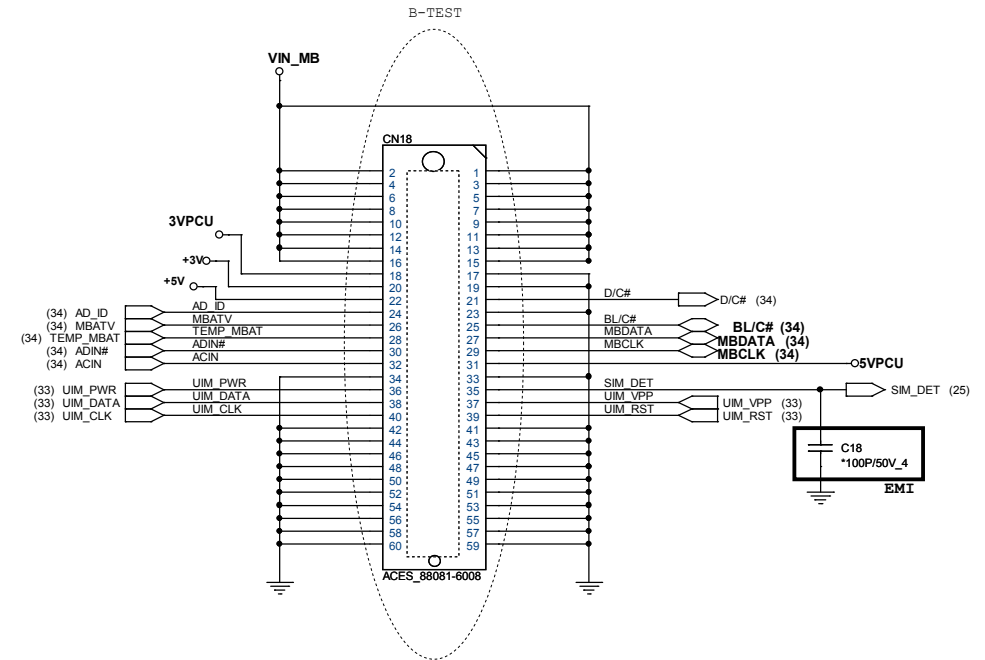
Board ID For Model	ID5 GPIO37	ID4 GPIO36
LE6	0	0
LE7	0	1
LE8	1	0
LE9	1	1
KL1	0	0





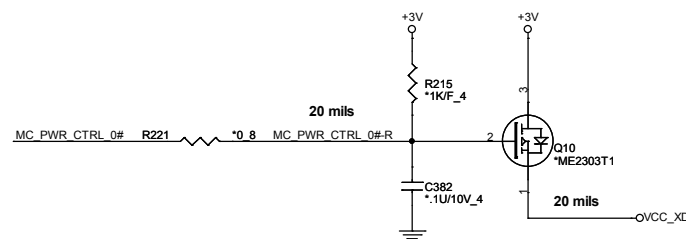
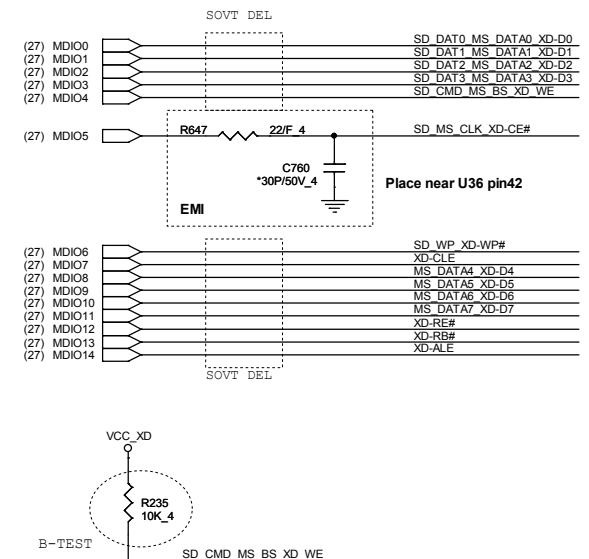
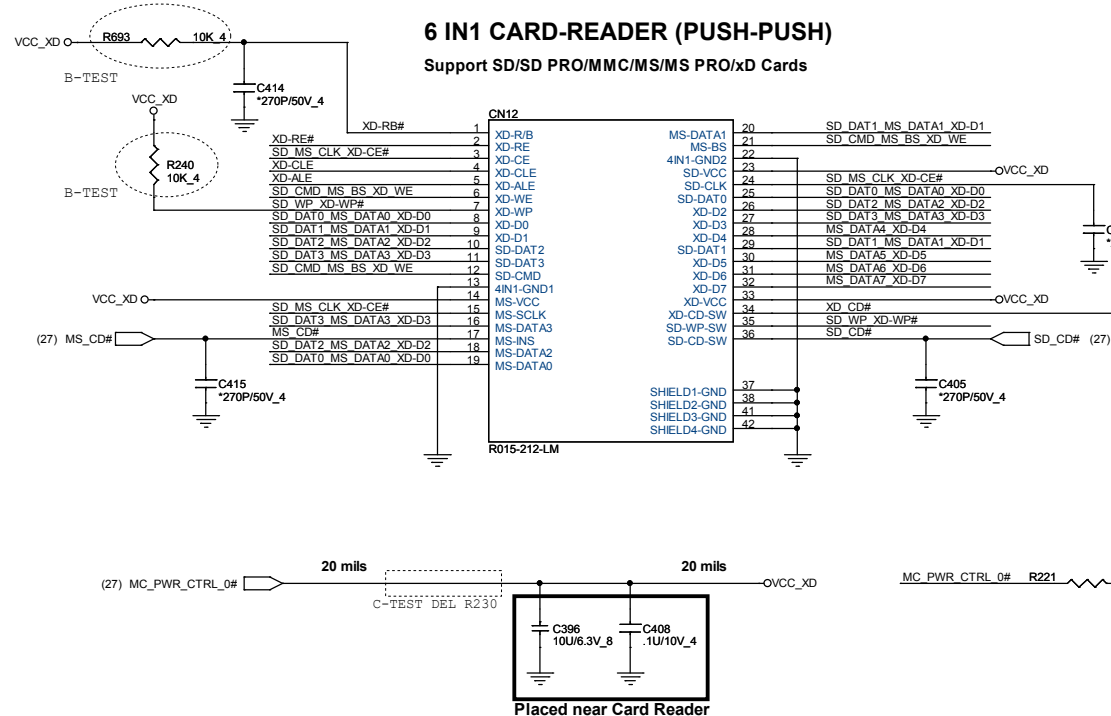



Charger+SIM CARD B to B 60PIN CONN

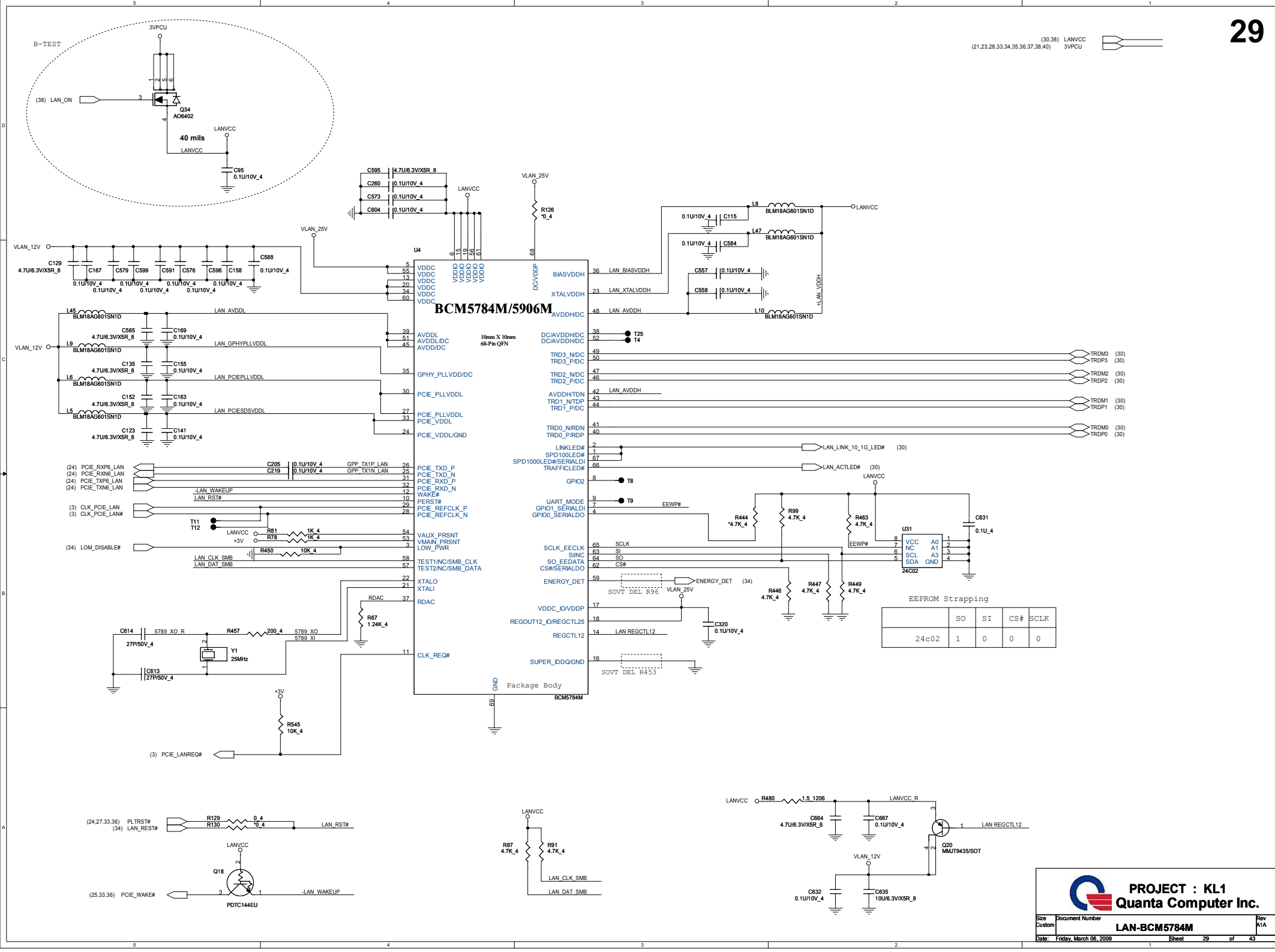
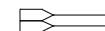


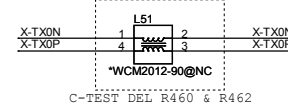
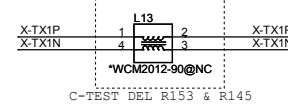
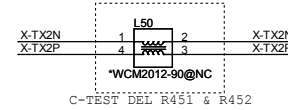
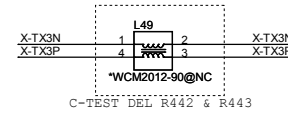
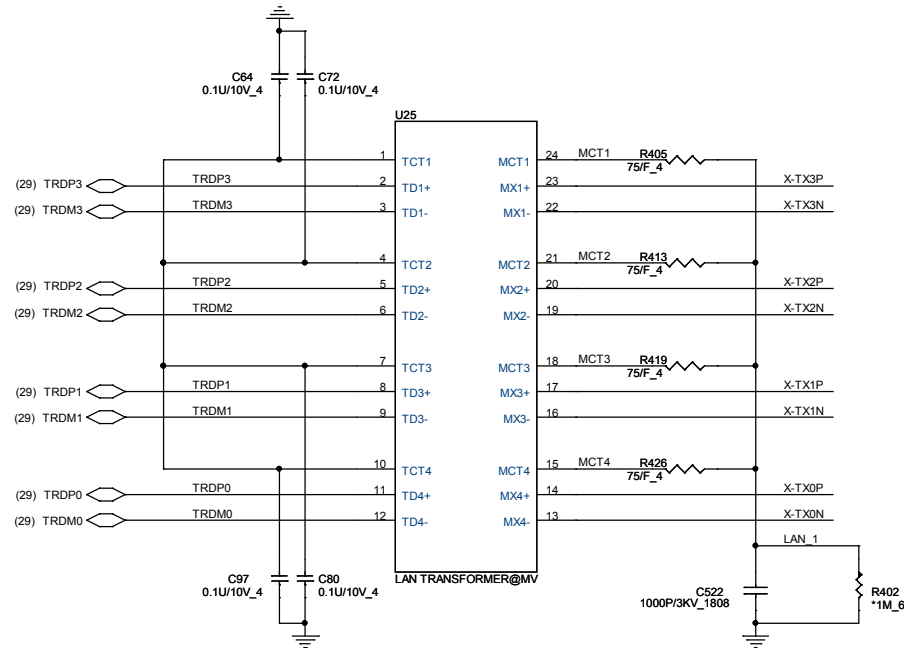
6 IN1 CARD-READER (PUSH-PUSH)

Support SD/SD PRO/MMC/MS/MS PRO/xD Cards

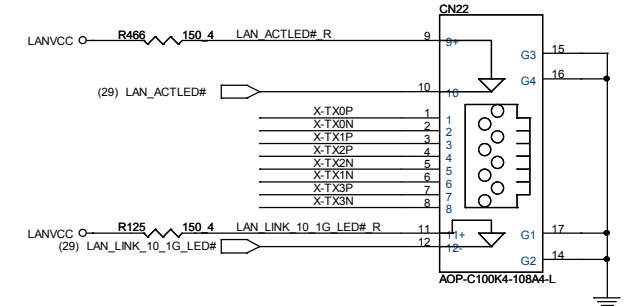


 PROJECT : KL1 Quanta Computer Inc.		
Size Custom	Document Number B to B CONN & CR SOCKET	Rev A1A
Date: Friday, March 06, 2009	Sheet 28 of 43	



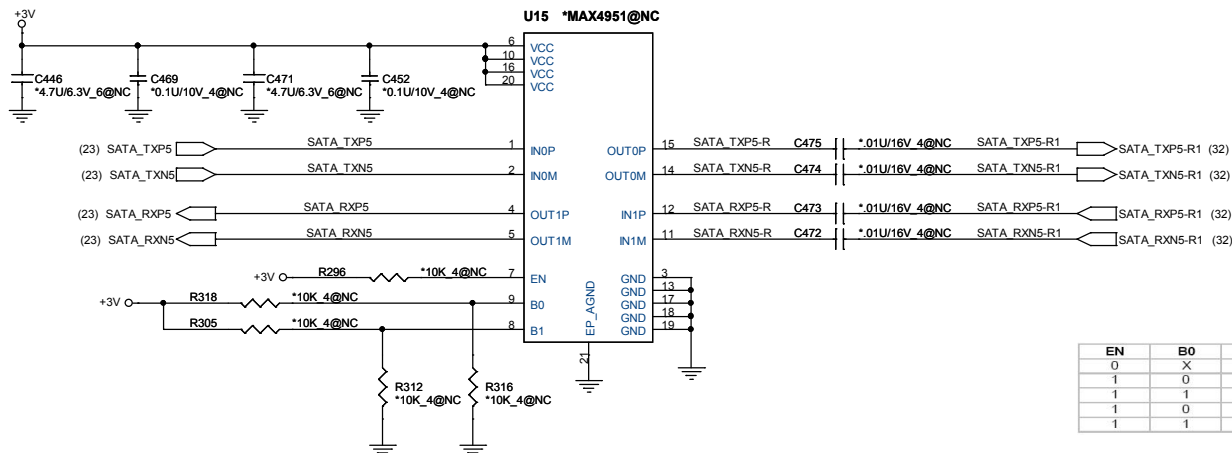


RJ45 CONN



E-SATA RE-DRIVER

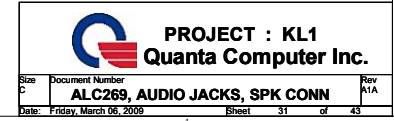
SATA_TXP5	R283	0 4	SATA_TXP5-R1
SATA_TXN5	R282	0 4	SATA_TXN5-R1
SATA_RXP5	R281	0 4	SATA_RXP5-R1
SATA_RXN5	R280	0 4	SATA_RXN5-R1



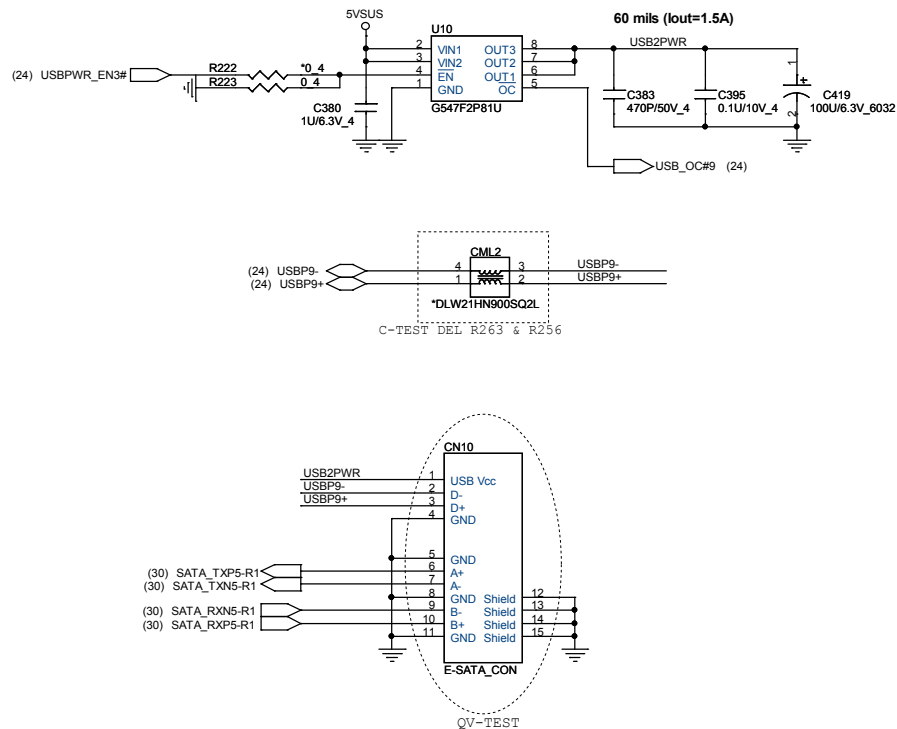
EN	B0	B1	FUNCTION
0	X	X	Standby
1	0	0	Standard SATA Output
1	1	0	Ch 0 Boost Output
1	0	1	Ch 1 Boost Output
1	1	1	Ch 0,1 Boost Output



PROJECT : KL1
Quanta Computer Inc.

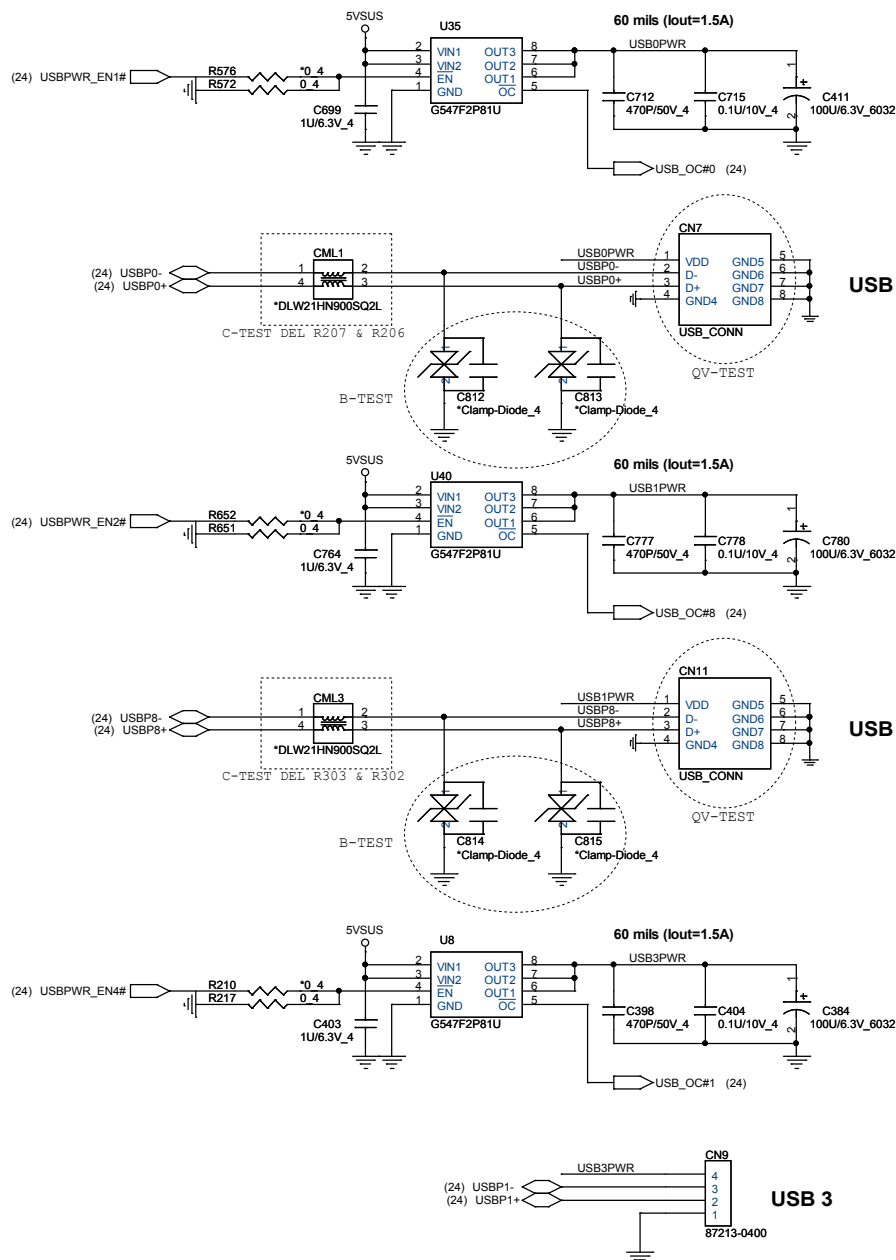


USB + eSATA CONNECTOR



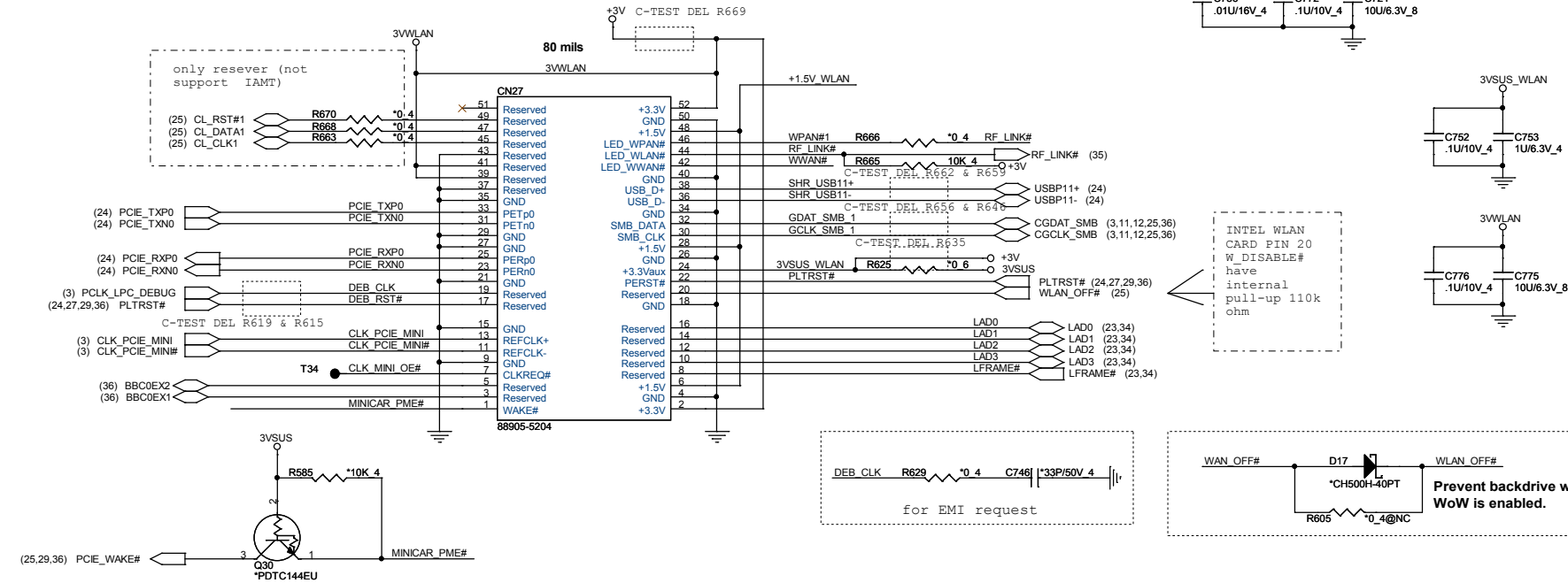
USBX3

32

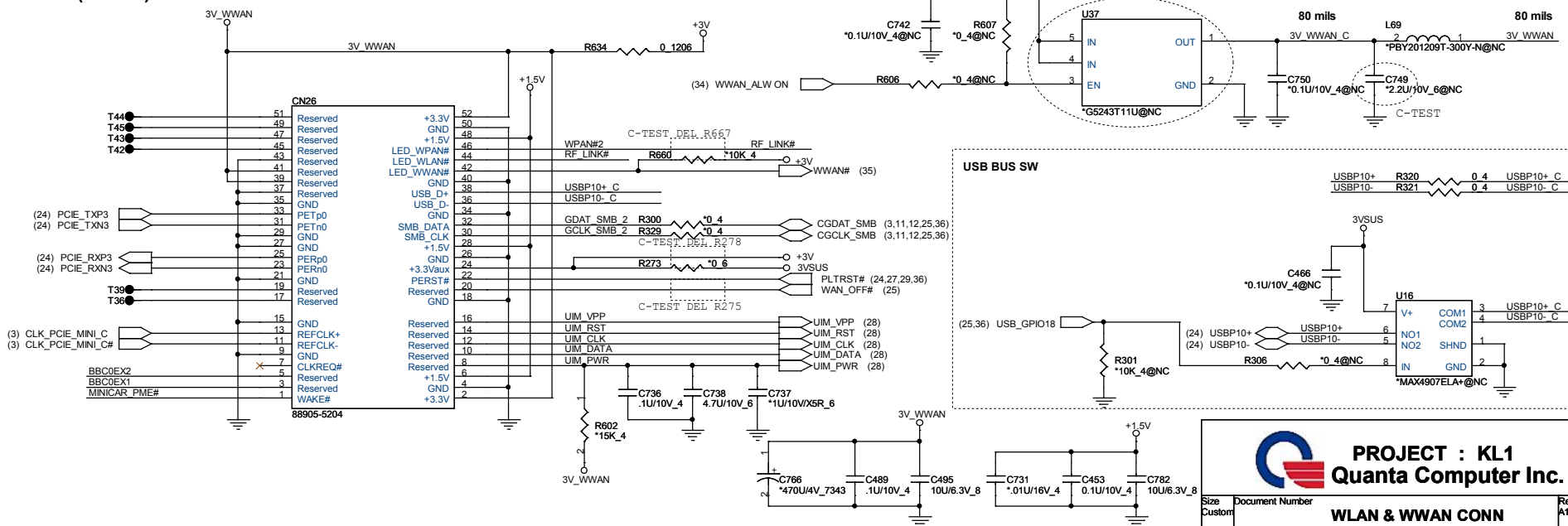


Mini PCI-E Card 1 WLAN

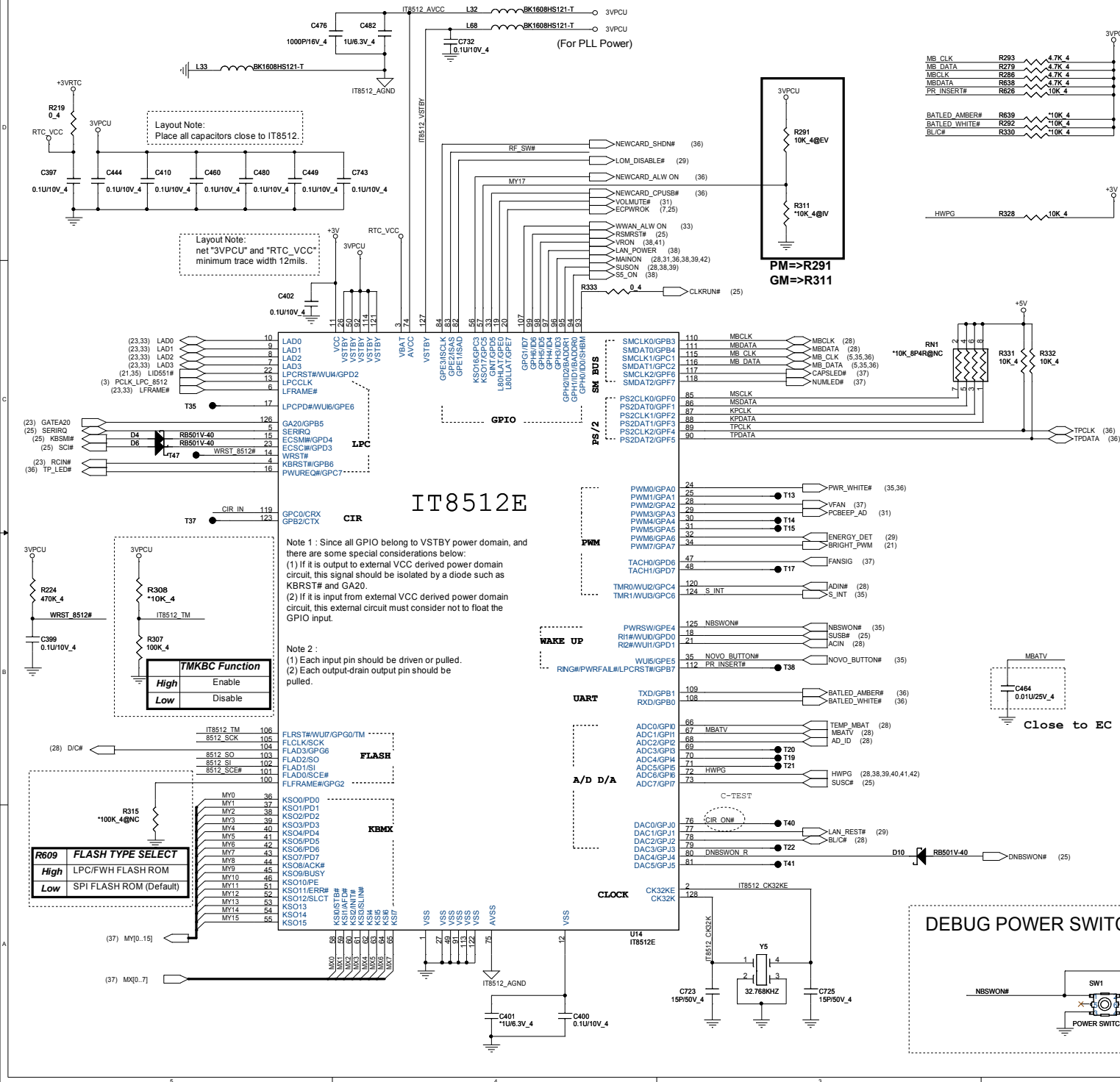
33



Mini PCI-E Card 2 WWAN(W/SIM)



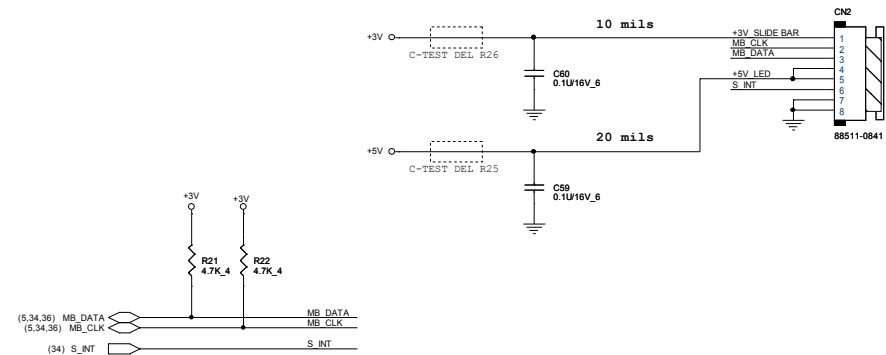
PROJECT : KL1
Quanta Computer Inc.



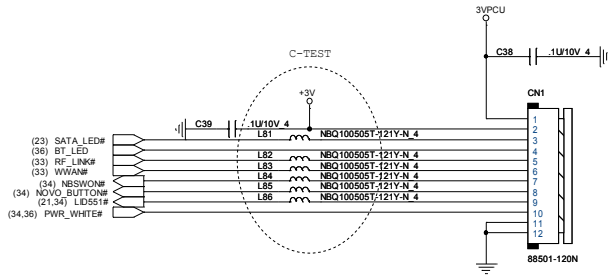
PROJECT : KL1
Quanta Computer Inc.

Size: Custom
Document Number: EC IT8512E
Date: Friday, March 06, 2009
Sheet: 34 of 43
Rev: A1A

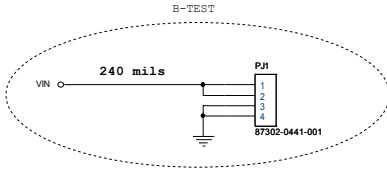
SLIDE BAR CONN



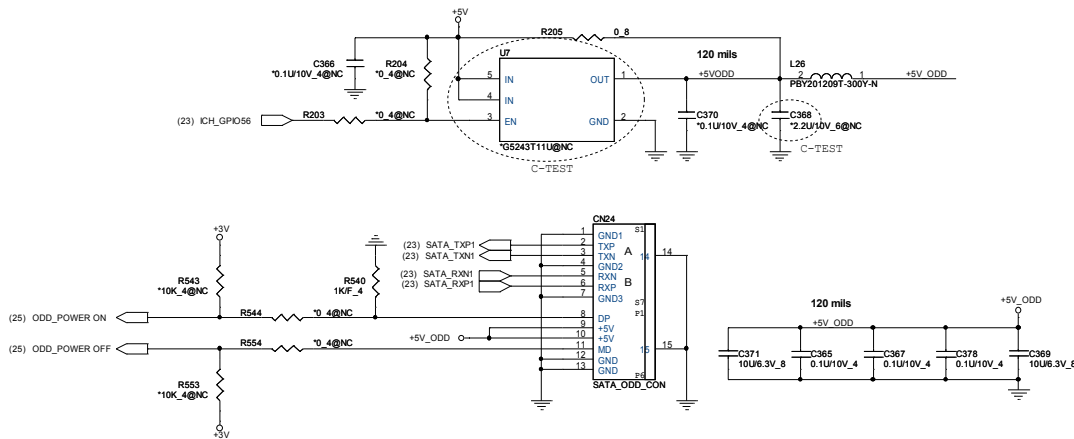
POWER BUTTON/B CONN



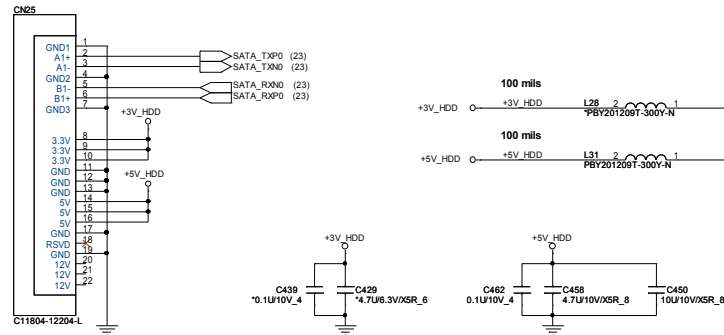
VIN CABLE CONN

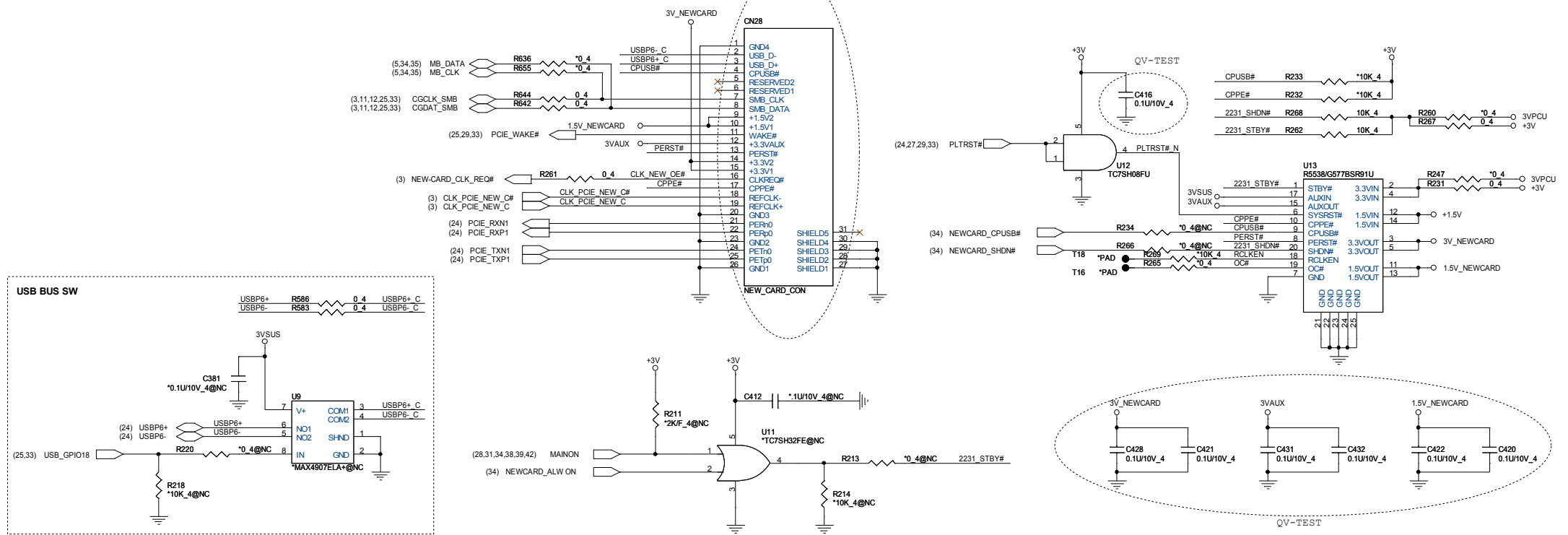


SATA CD-ROM

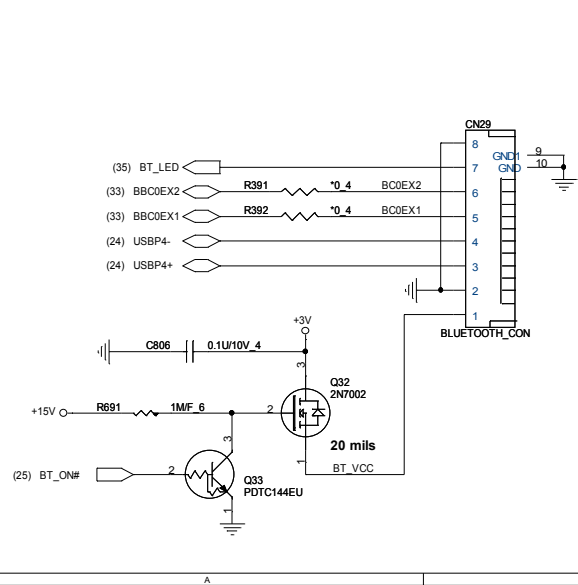


SATA-HDD CONNECTOR

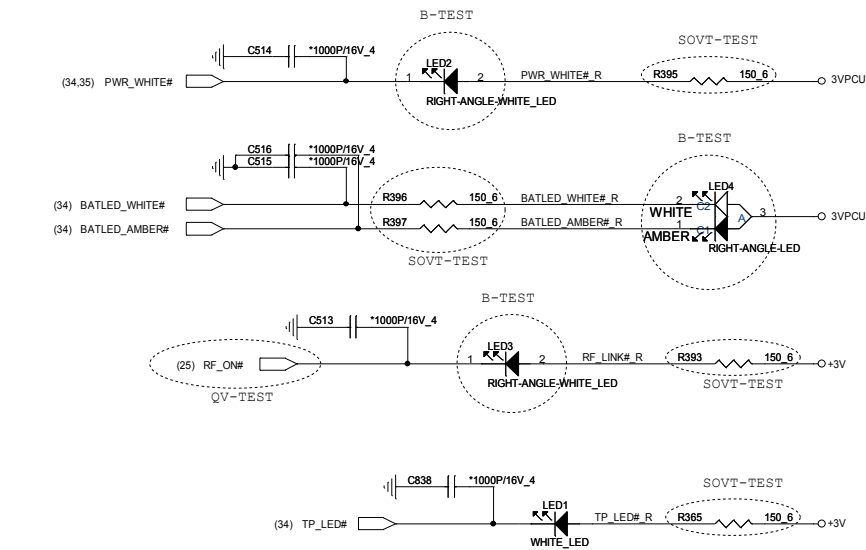




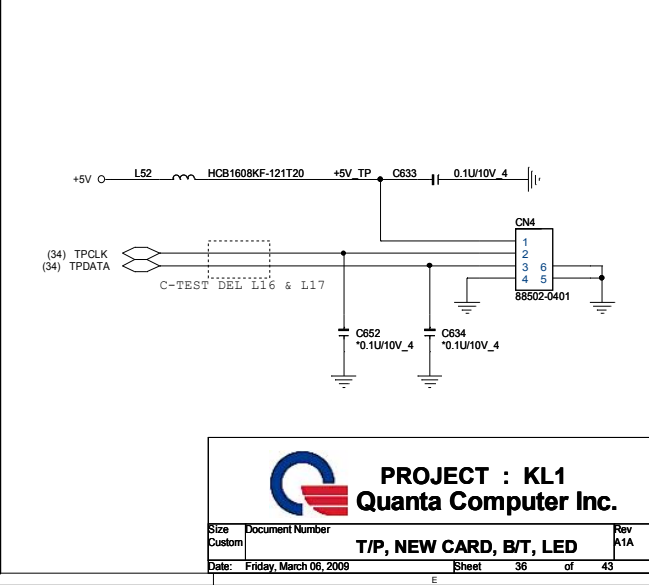
BLUETOOTH



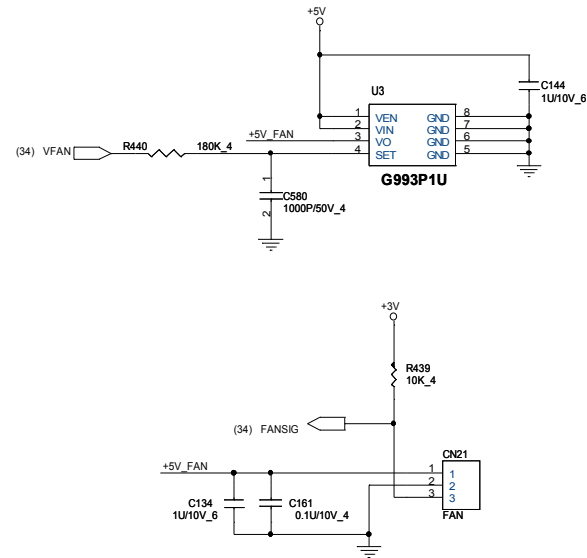
LED



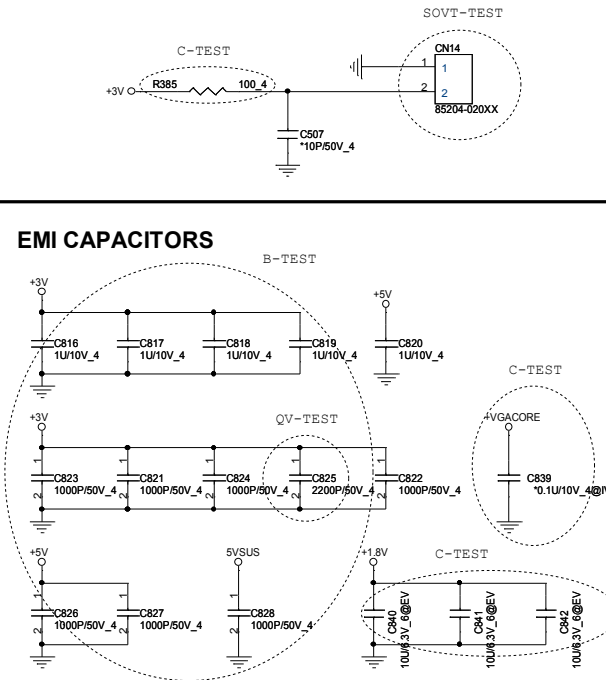
TOUCH PAD



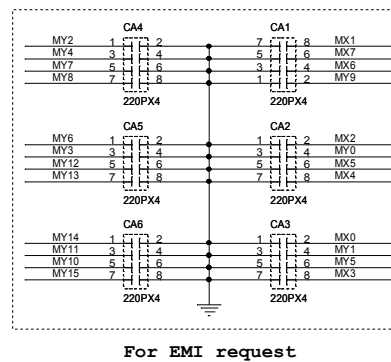
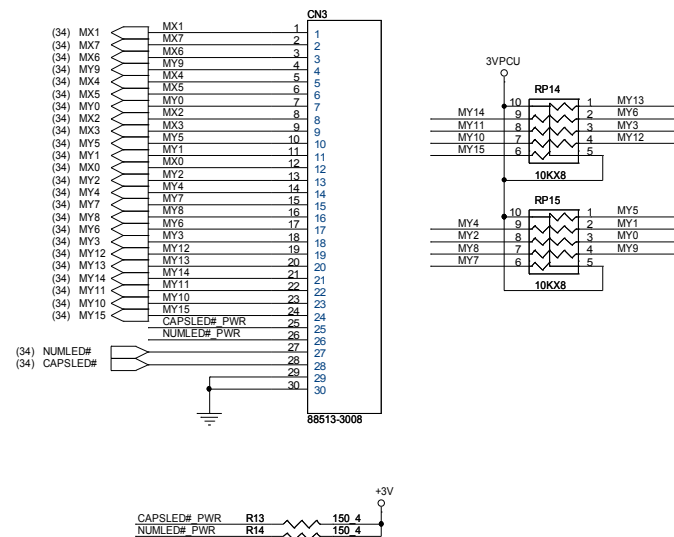
FAN CONTROL



Logo LED CONN

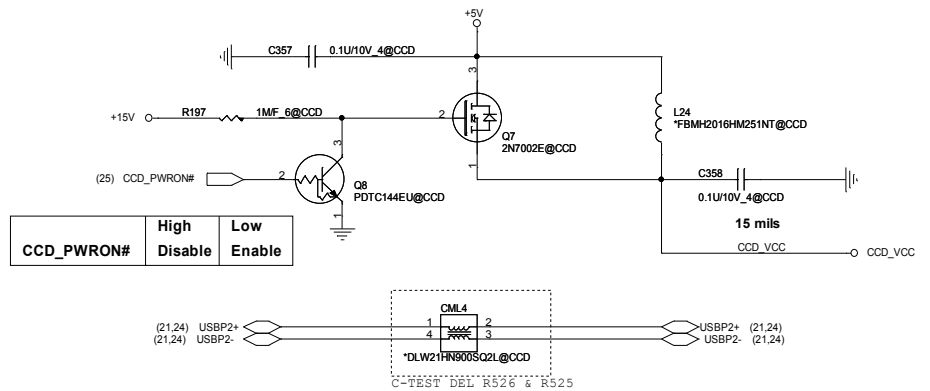


KEYBOARD

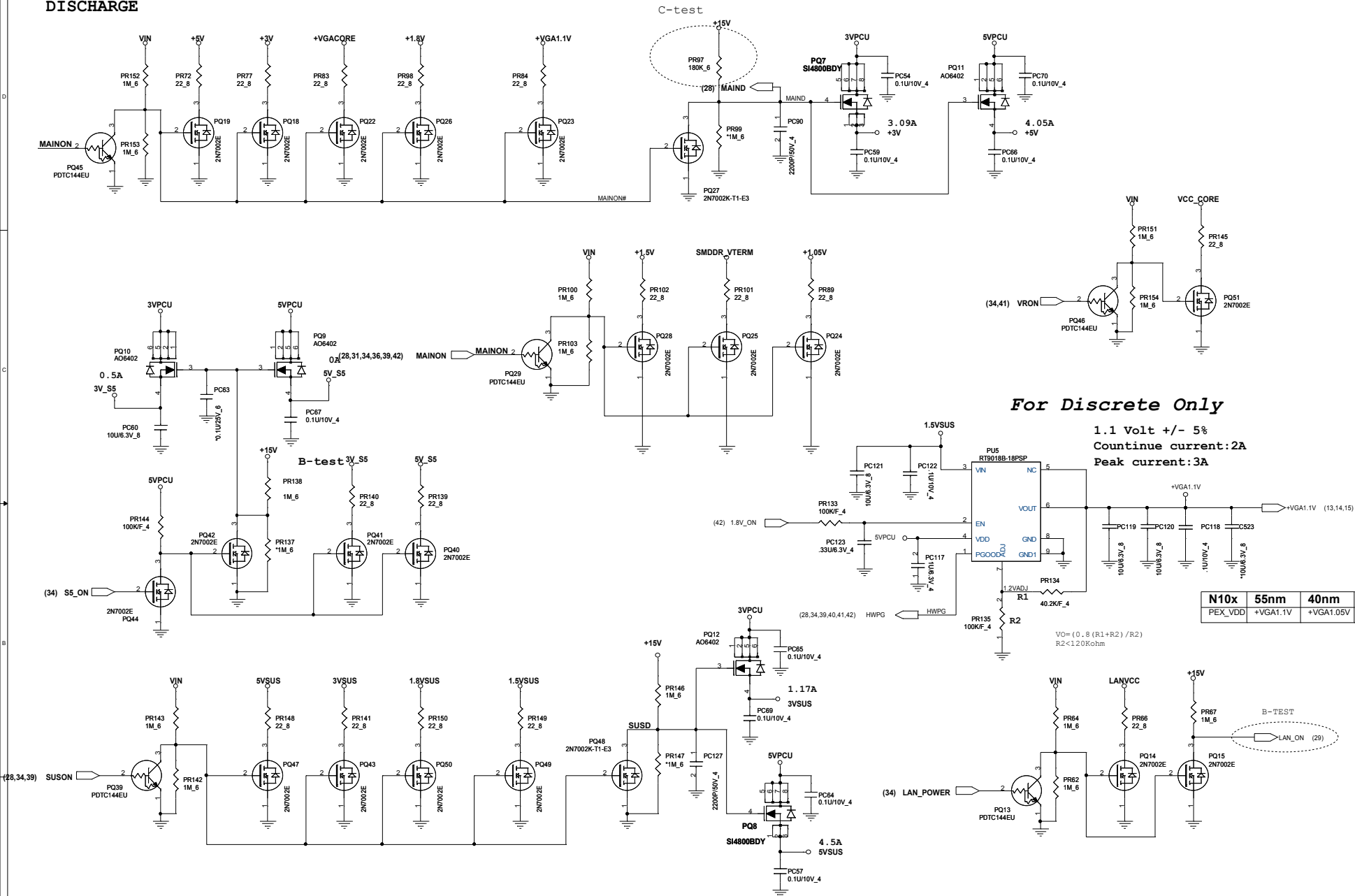


For EMI request

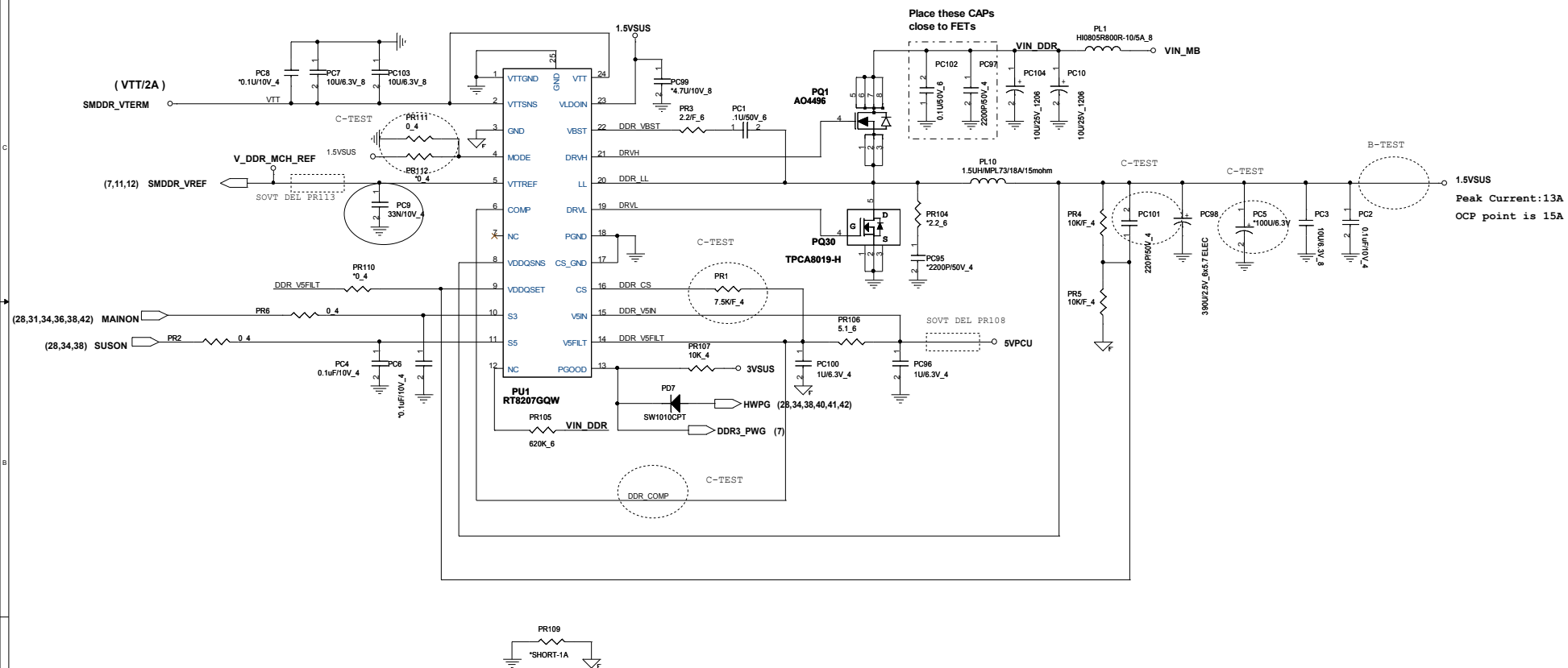
CCD MODULE



DISCHARGE



PROJECT : KL1
Quanta Computer Inc.



DC/DC 3VPCU/5VPCU/+15V

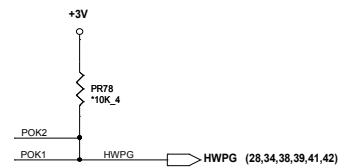
Ton:OUT1/OUT2 Switching Frequency
 VCC: 200kHz/300kHz
 OPEN (REF): 400kHz/300kHz
 GND: 400kHz/500kHz

Peak Current: 6A
 OCP point: 7.5A

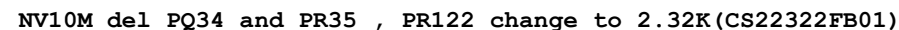
Peak Current: 7A
 OCP point: 9A

REFIN2: DYNAMIC 0 to 2V
 REFIN2 = RTC: 1.05V Fixed
 REFIN2 = VCC: 3.3V Fixed


LDO = 5V (LDOREFIN = GND) or
 LDOREFIN RANGE: 0.3V to 2V
 LDO = 2x LDOREFIN



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N10x	VGA_GPIO6 GPIO6	V_PWRCNTL GPIO5	PERFORMANCE STATE	N10P-GE1	N10M-GS1
55nm	Low	Low	HD DVD/SD DVD/MAX BAT	0.9V	0.9V
	High	High	MAX PERFORMANCE	1.10V	0.92V
40nm					

 <div style="display: inline-block; vertical-align: middle;"> <p>PROJECT : KL1</p> <p>Quanta Computer Inc.</p> </div>	
Size B	<div style="display: flex; justify-content: space-between;"> <div>Document Number</div> <div>VGA Core (OZ8119)</div> <div>Rev A1A</div> </div>
Date:	<div style="display: flex; justify-content: space-between;"> <div>Friday, March 06, 2009</div> <div>Sheet 42 of 43</div> </div>

KL1 SYSTEM POWER BLOCK DIAGRAM

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